Greetings from

IPC and Georgia Tech

Managing Power Integrity
Status, Challenges and Opportunities

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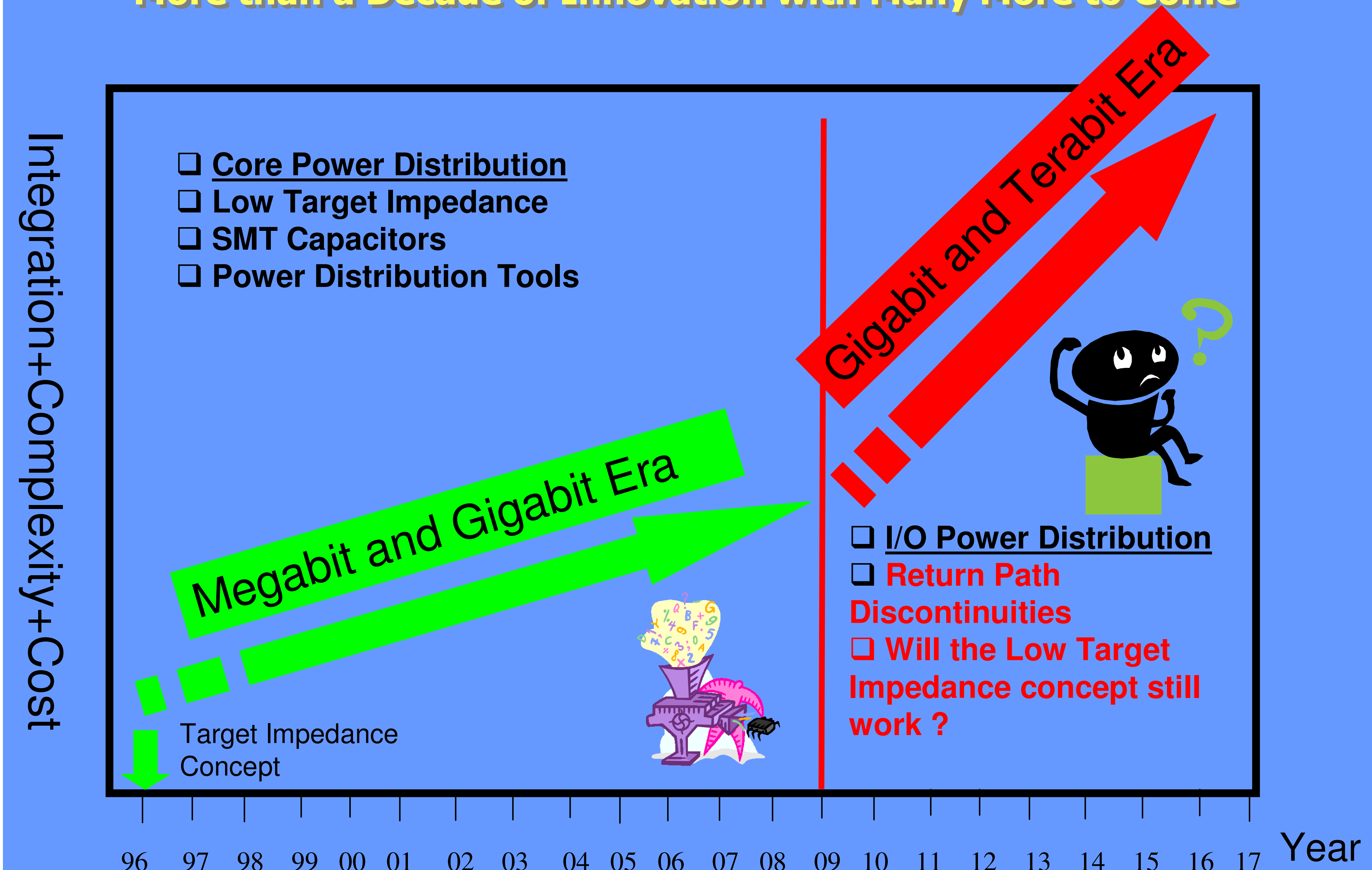
an SRC Center of Excellence at Georgia Tech

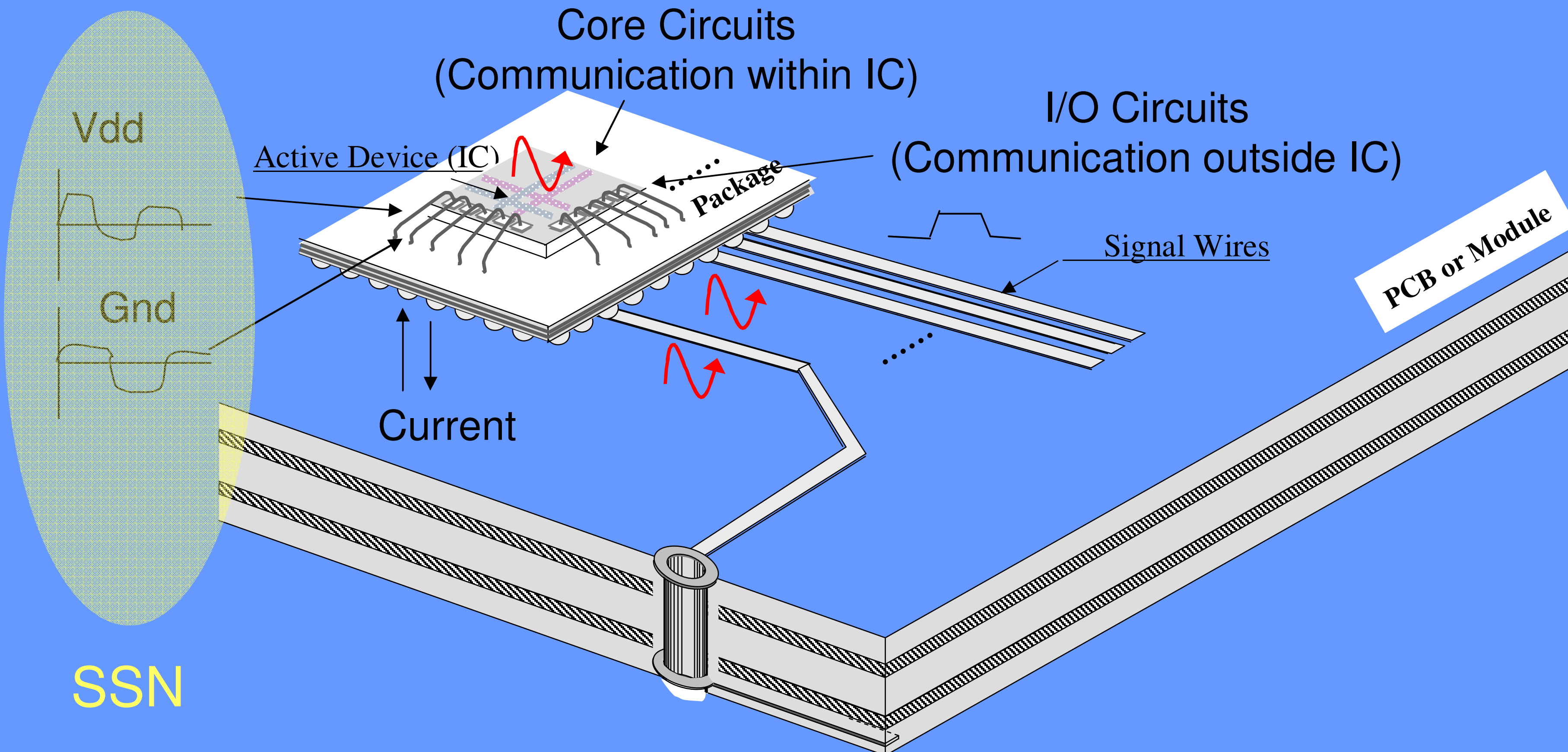
Outline

- Motivation
- Overview of the past (Boring)
- Challenges and Opportunities for the Future (most Interesting)

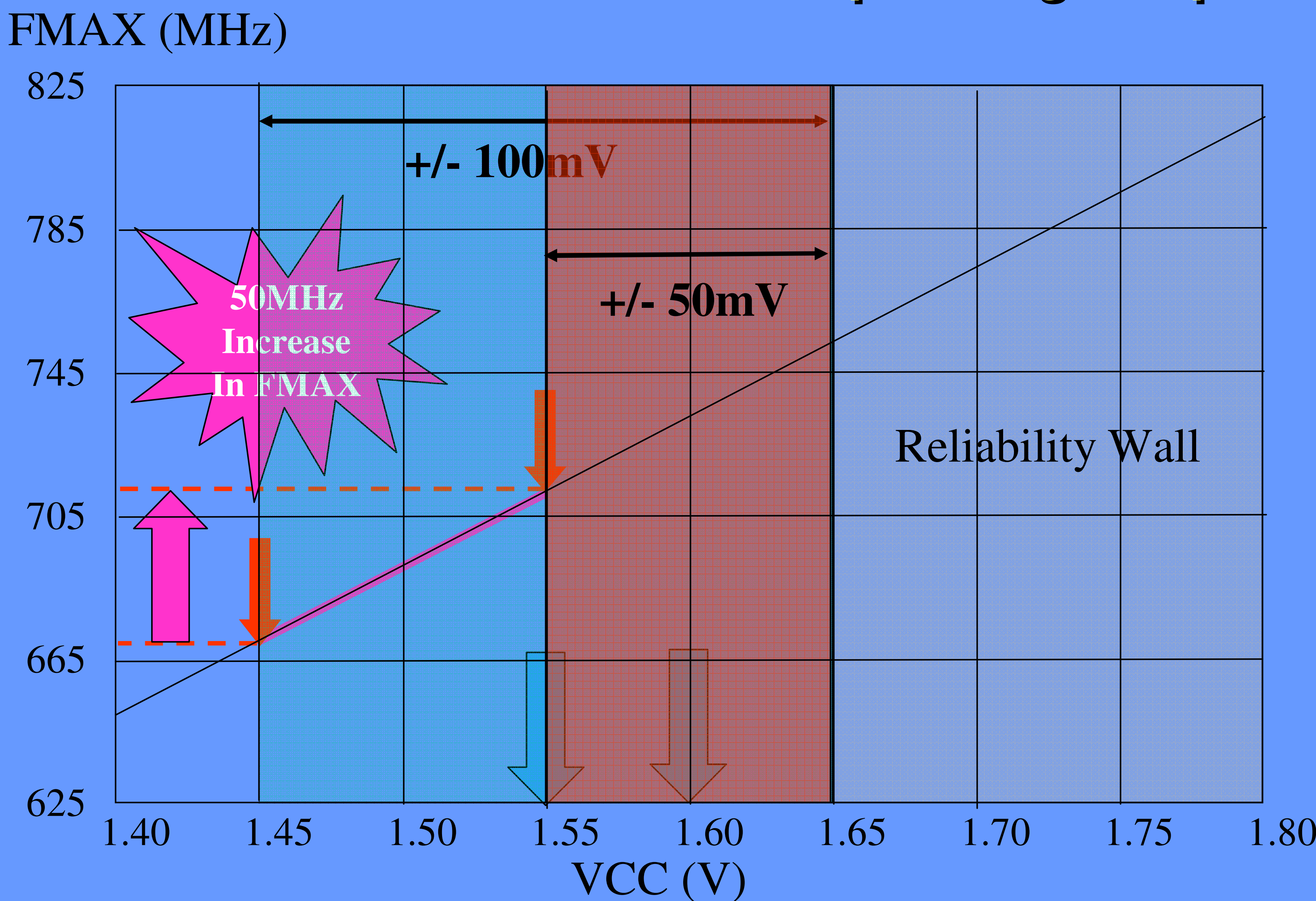
Power Distribution
More than a Decade of Innovation with Many More to Come



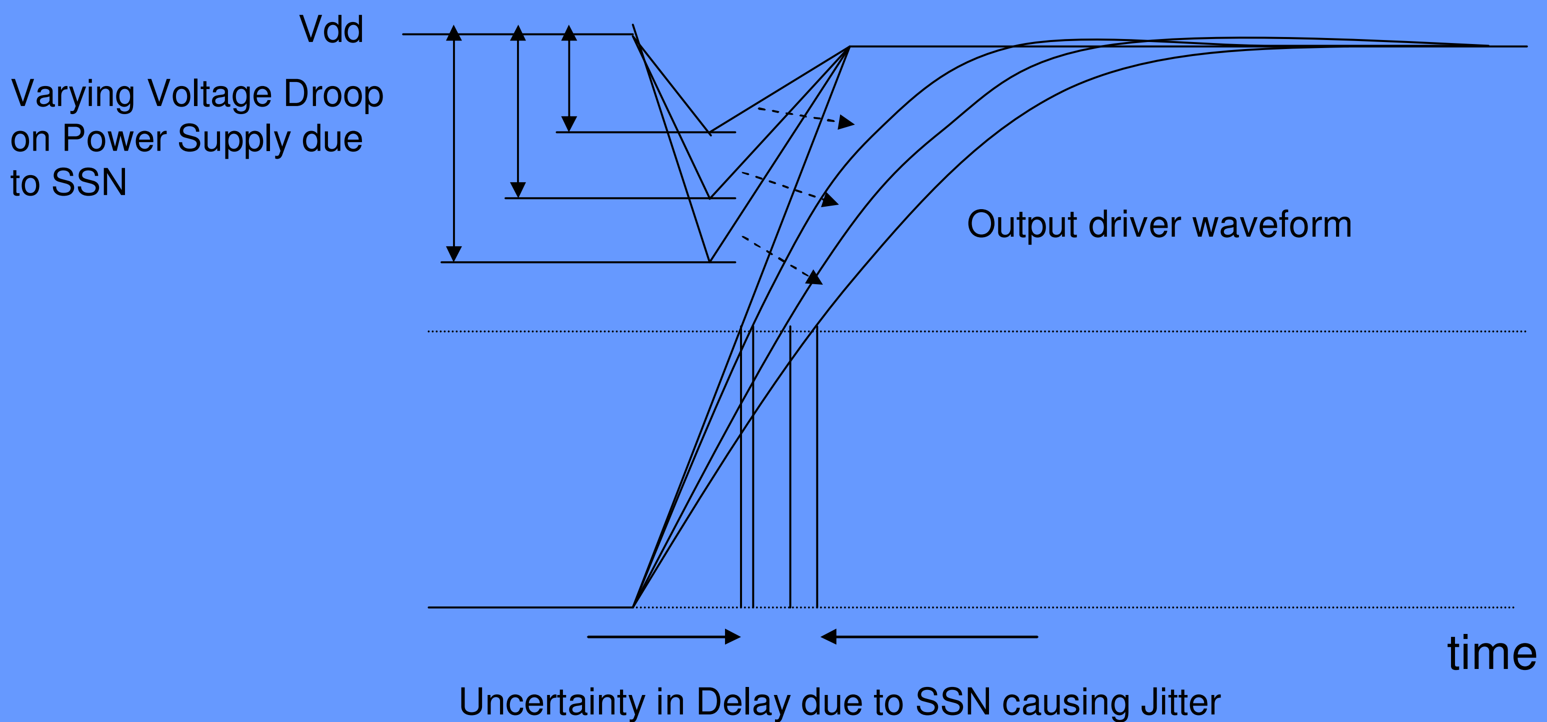
SSN in High-Speed / High-I/O Packages and High-Speed Boards



Power Distribution Affects Operating Frequency

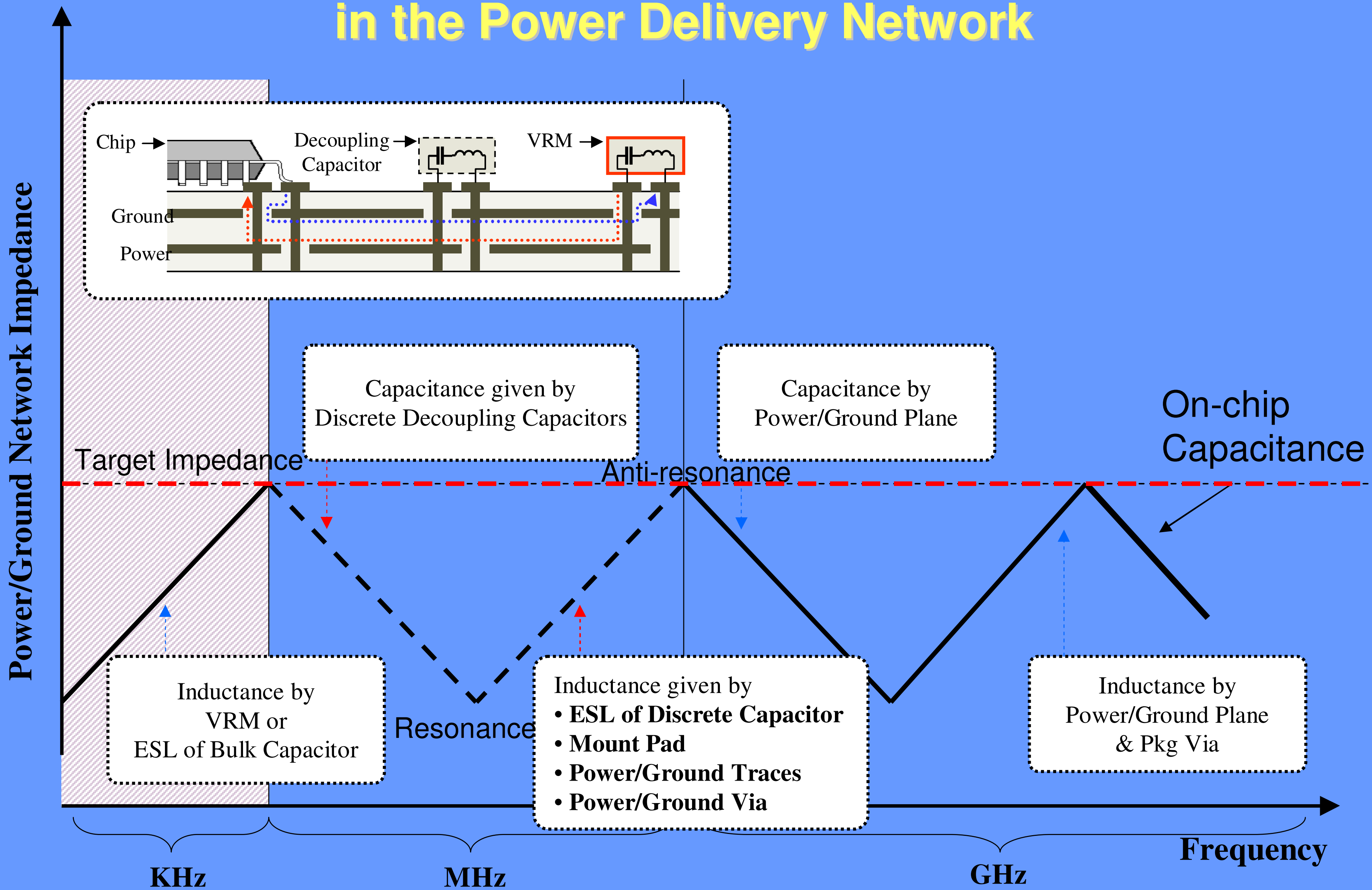


SSN causes Jitter



Courtesy: Sony

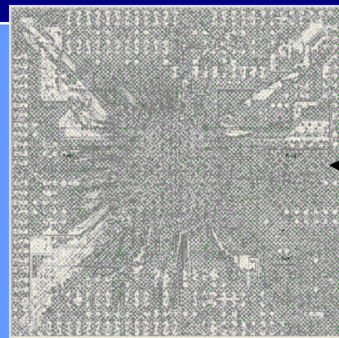
Impedance Vs Frequency and the role of various components in the Power Delivery Network



Courtesy: Prof. J. Kim, KAIST, S. Korea and Ansoft Corporation

Signal and Power Integrity Modeling

CAD Layout of Package and PCB



Courtesy: E-System Design (www.e-systemdesign.com)

Fix Frequency Response

Frequency Domain

Evaluate Layout
- Signal RL and IL
- Substrate Coupling
- PDN Impedance
- SSN

Fix DC Drop

DC Modeling of PDN

Evaluate DC Drops
- Voltage distribution

AC Modeling of Signal and Power Distribution

Fix Voltage & Timing Margin

Frequency to Time Conversion

Create
- Spice Sub-circuit of frequency response

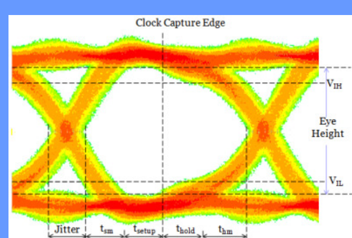
Macro-modeling

Time Domain

Evaluate Drv/Rcv Path
- Driver Non-linearity
- Eye Diagrams
  - Timing Margin
  - Voltage Margin

Transient Simulation

Acceptable Output Eye Diagram



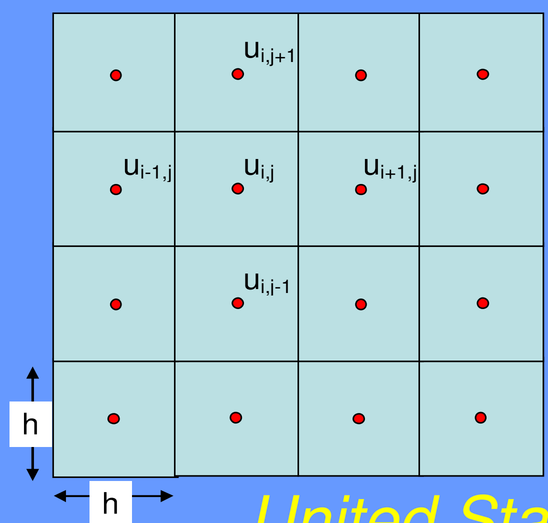
Multi-layered Finite Difference Method (M-FDM)
High Frequency Signal and Power Integrity Analysis

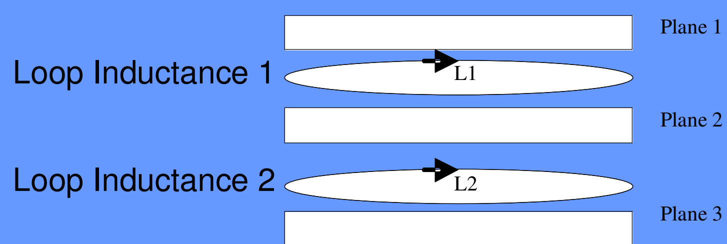
- Helmholtz Equation (Differential Form)

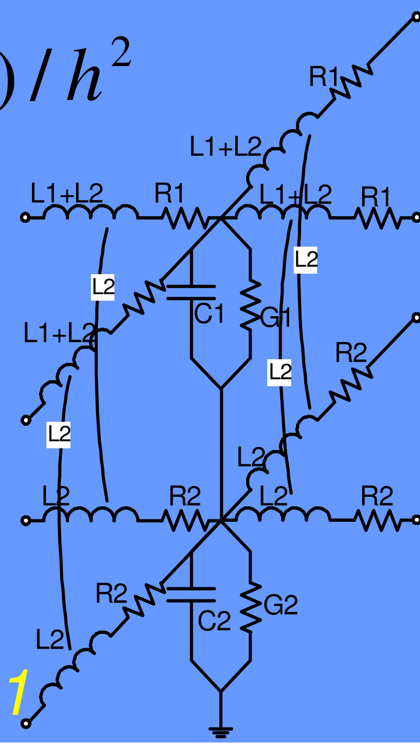
$$(\nabla_T^2 + k^2)u = -j\omega\mu dJ_z$$

- Five point Finite Difference Approximation

$$\nabla_T^2 u_{i,j} = (u_{i,j-1} + u_{i,j+1} + u_{i-1,j} + u_{i+1,j} - 4u_{i,j})/h^2$$



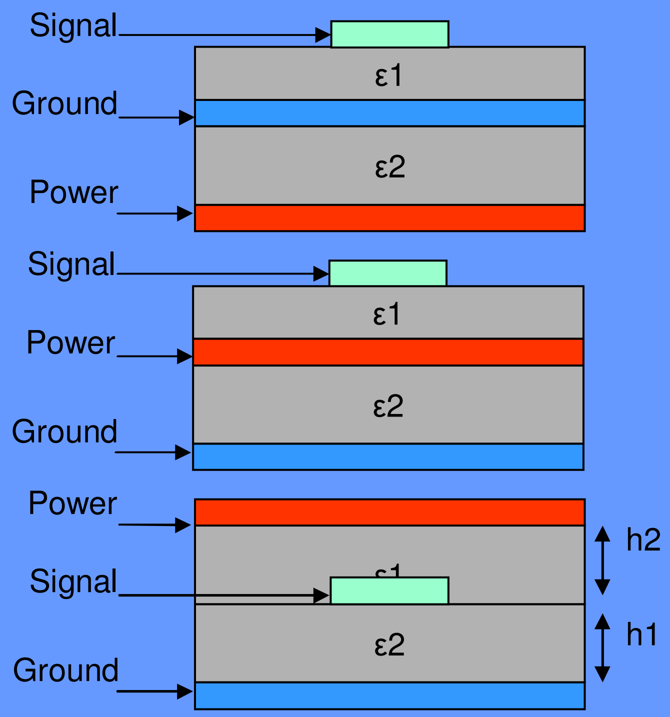


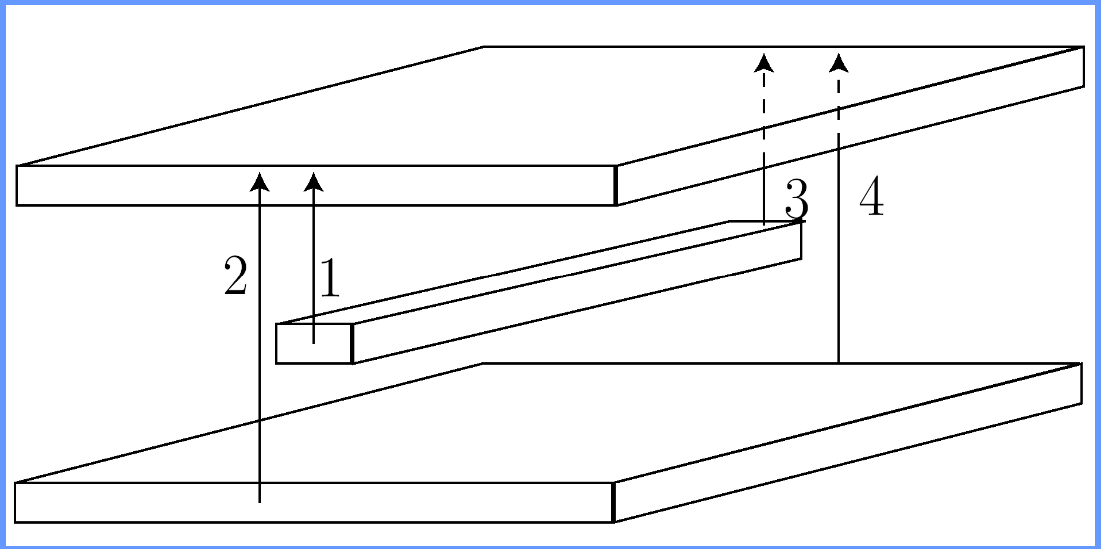


United States Patent 7,895,540, 2/22/11

Coupling to Signal lines

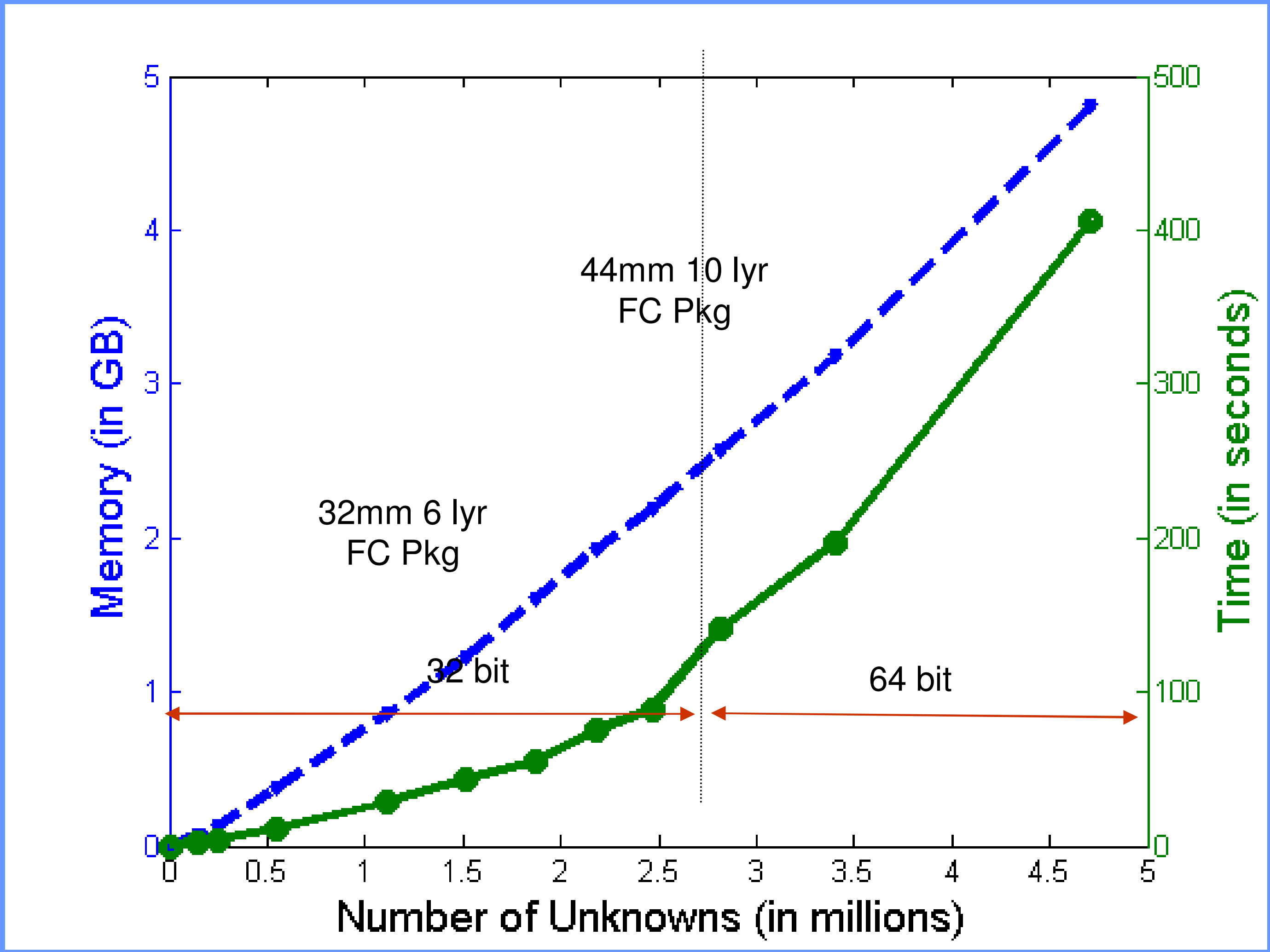
- Proprietary Signal Referencing Method
- Preserves sparse matrix
- Model return currents and coupling





Courtesy: E-System Design (www.e-systemdesign.com)

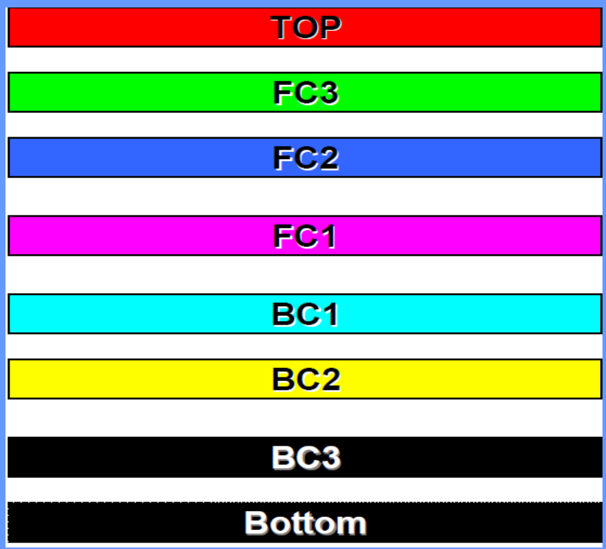
Scalability, Memory and Timing

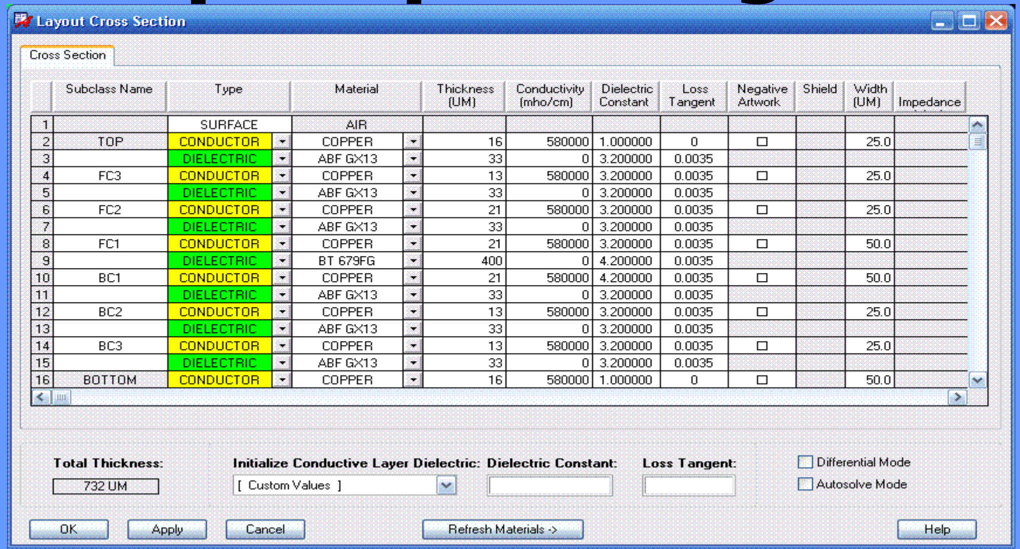


Note: Time per frequency point

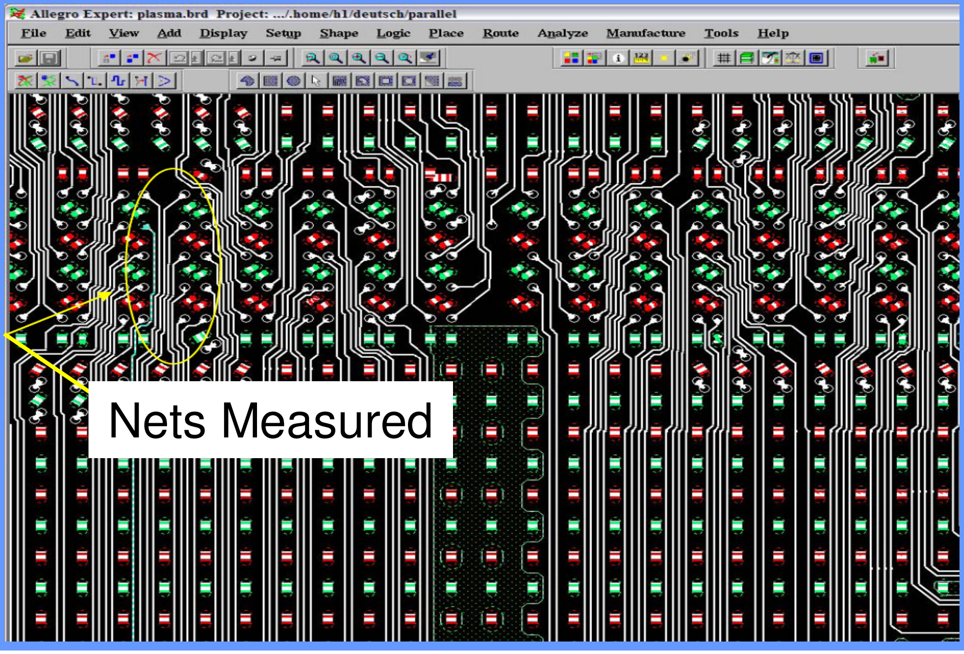
Sphinx for Signoff: www.e-systemdesign.com

IBM 8 Layer Flip Chip Package





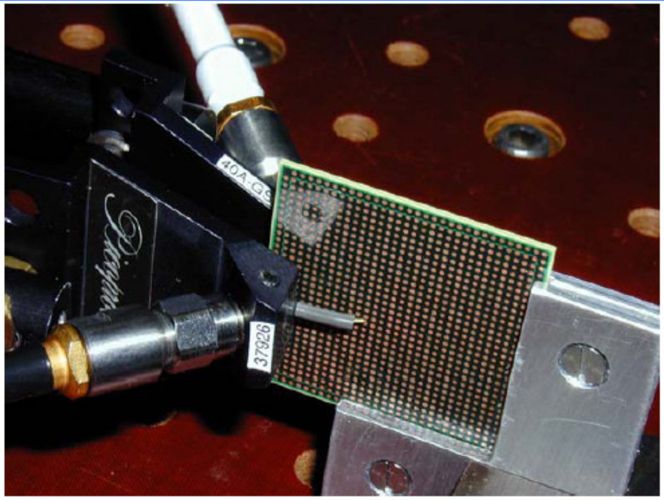
	Subclass Name	Type	Material	Thickness (UM)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (UM)	Impedance
1		SURFACE	AIR								
2	TOP	CONDUCTOR	COPPER	16	580000	1.000000	0	☐		25.0	
3		DIELECTRIC	ABF GX13	33	0	3.200000	0.0035				
4	FC3	CONDUCTOR	COPPER	13	580000	3.200000	0.0035	☐		25.0	
5		DIELECTRIC	ABF GX13	33	0	3.200000	0.0035				
6	FC2	CONDUCTOR	COPPER	21	580000	3.200000	0.0035	☐		25.0	
7		DIELECTRIC	ABF GX13	33	0	3.200000	0.0035				
8	FC1	CONDUCTOR	COPPER	21	580000	3.200000	0.0035	☐		50.0	
9		DIELECTRIC	BT 679FG	400	0	4.200000	0.0035				
10	BC1	CONDUCTOR	COPPER	21	580000	4.200000	0.0035	☐		50.0	
11		DIELECTRIC	ABF GX13	33	0	3.200000	0.0035				
12	BC2	CONDUCTOR	COPPER	13	580000	3.200000	0.0035	☐		25.0	
13		DIELECTRIC	ABF GX13	33	0	3.200000	0.0035				
14	BC3	CONDUCTOR	COPPER	13	580000	3.200000	0.0035	☐		25.0	
15		DIELECTRIC	ABF GX13	33	0	3.200000	0.0035				
16	BOTTOM	CONDUCTOR	COPPER	16	580000	1.000000	0	☐		50.0	

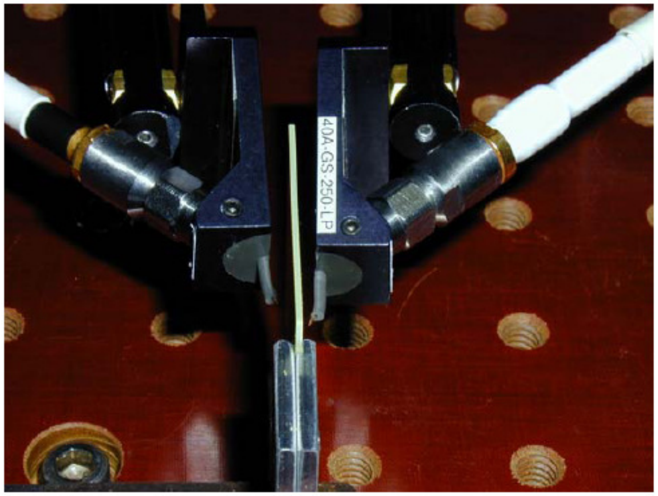


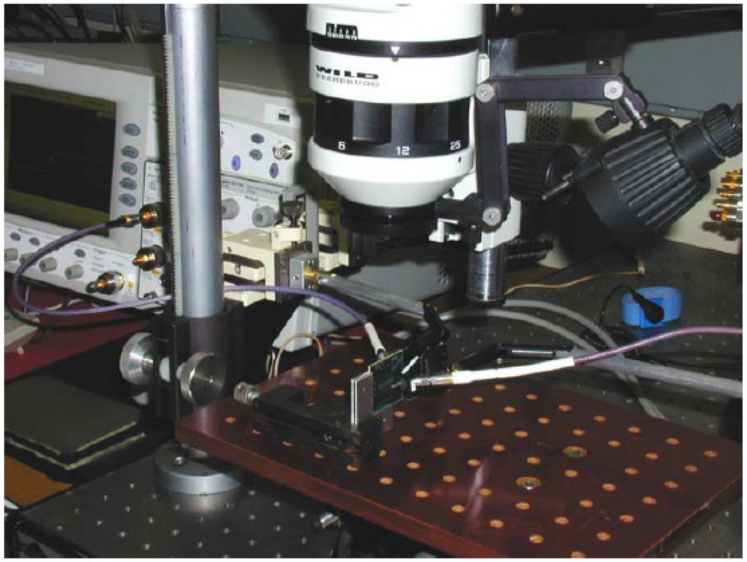
- ❑ Objectives
- ❑ Correlate Risetime, Delay NEXT and FEXT for the IBM Package
- ❑ All measurements done by IBM using TDR with top and bottom side probing

Courtesy: Alina Deutsch and Jason Morsey
IBM Yorktown Heights

Measurement Set-up



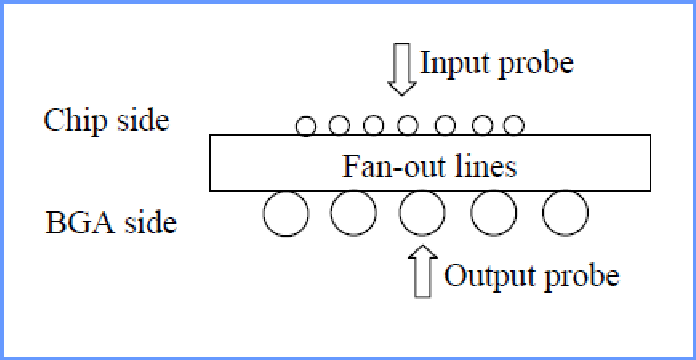


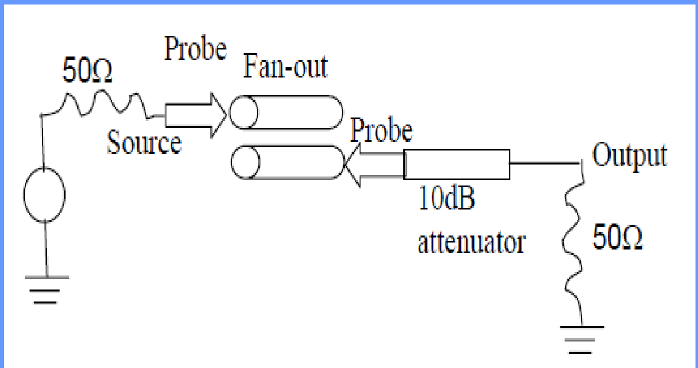


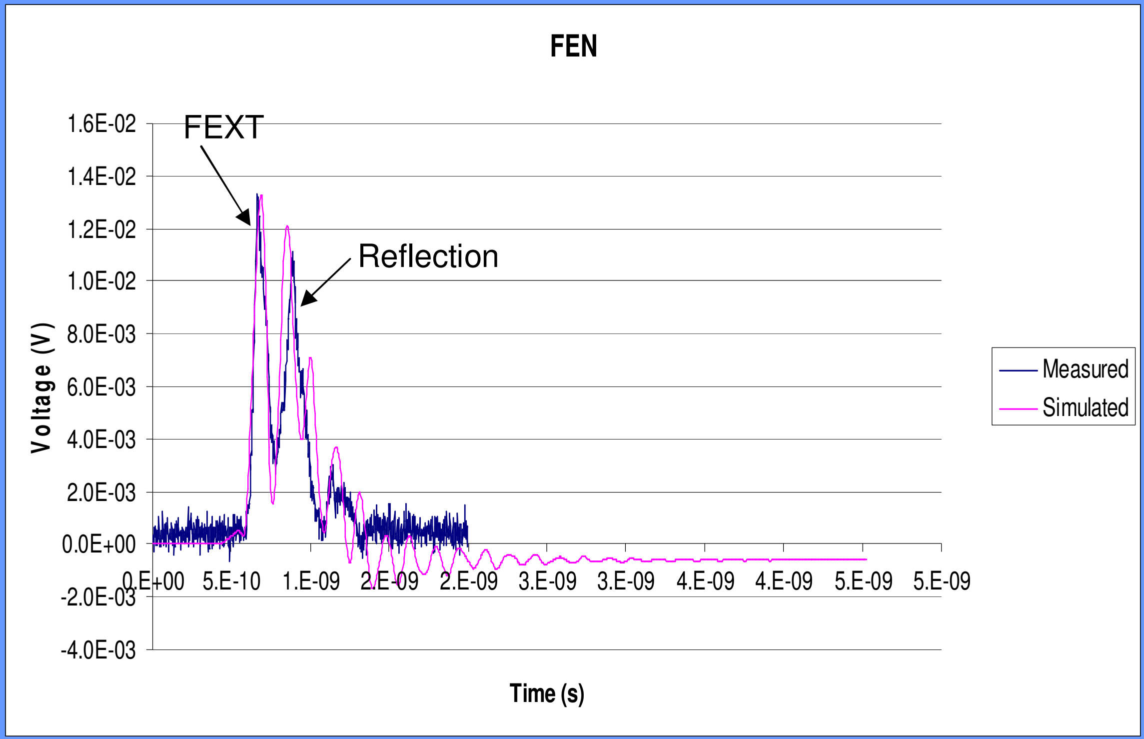
- TDR/TDT Set-up with 40ps pulse transition
- High Frequency probes and cables used

Courtesy: Alina Deutsch and Jason Morsey
IBM Yorktown Heights

Far End Cross Talk (FEXT)
Model to Hardware Correlation

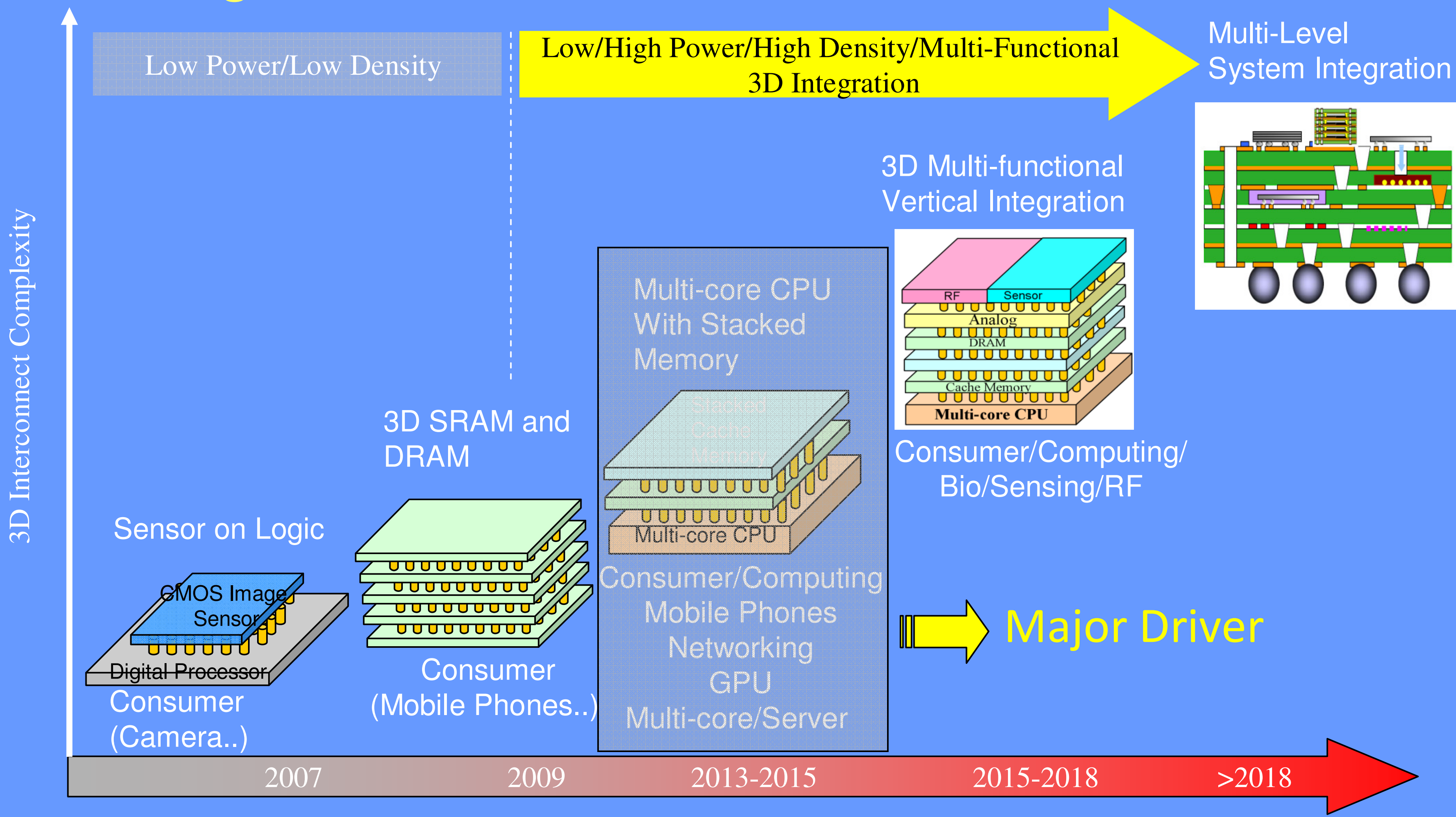




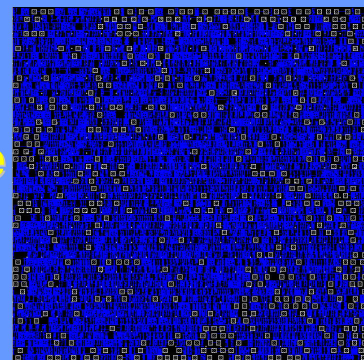


Parameter	Measurement	Sphinx
FEXT Amplitude	13.3mV	12.1mV

Interconnect and Packaging Center: Vision and Roadmap to Achieving Integration using 3D IC and Packaging Technologies



Coupling of Electrical, Thermal and Mechanical Effects
A Multi-Physics and Multi-scale Challenge

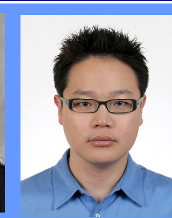


Place & Route

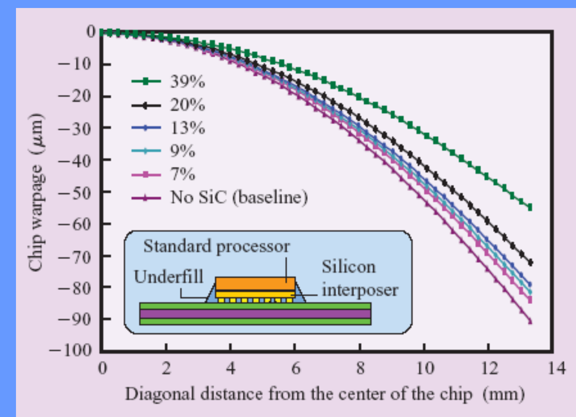
ECE

ME

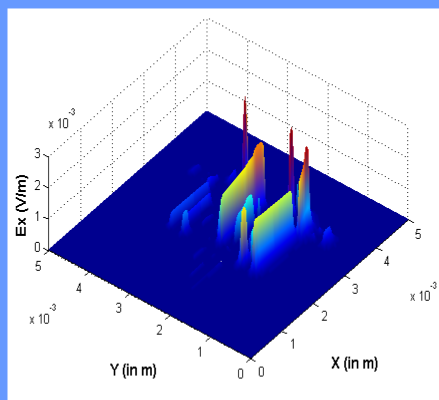
ME



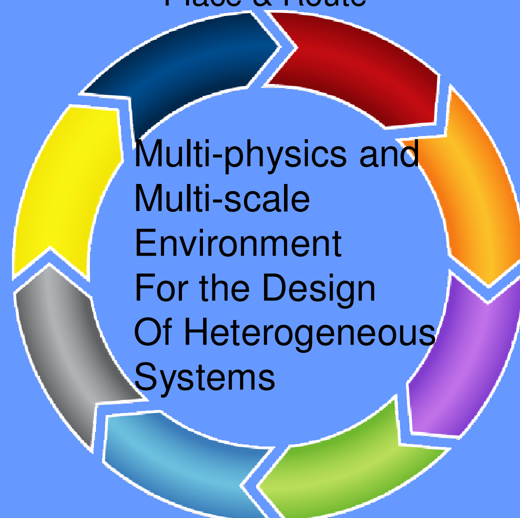
ECE

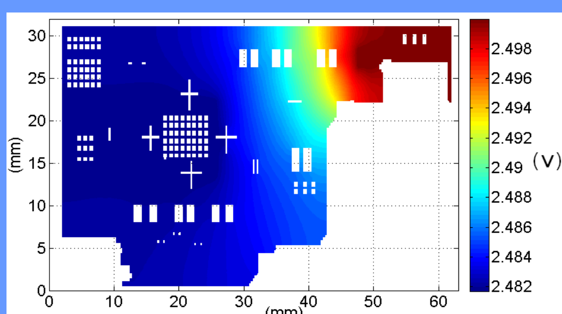


Mechanical Stresses

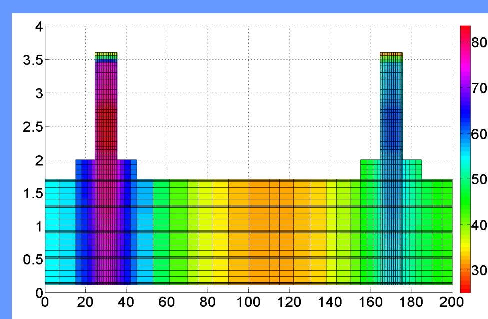


Signal Integrity

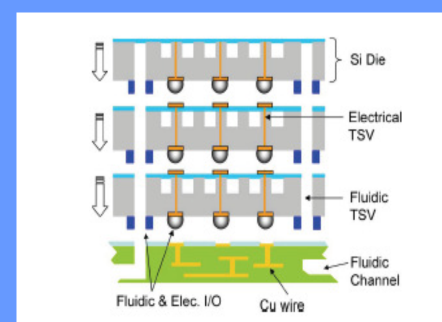




Power Delivery/DC/AC

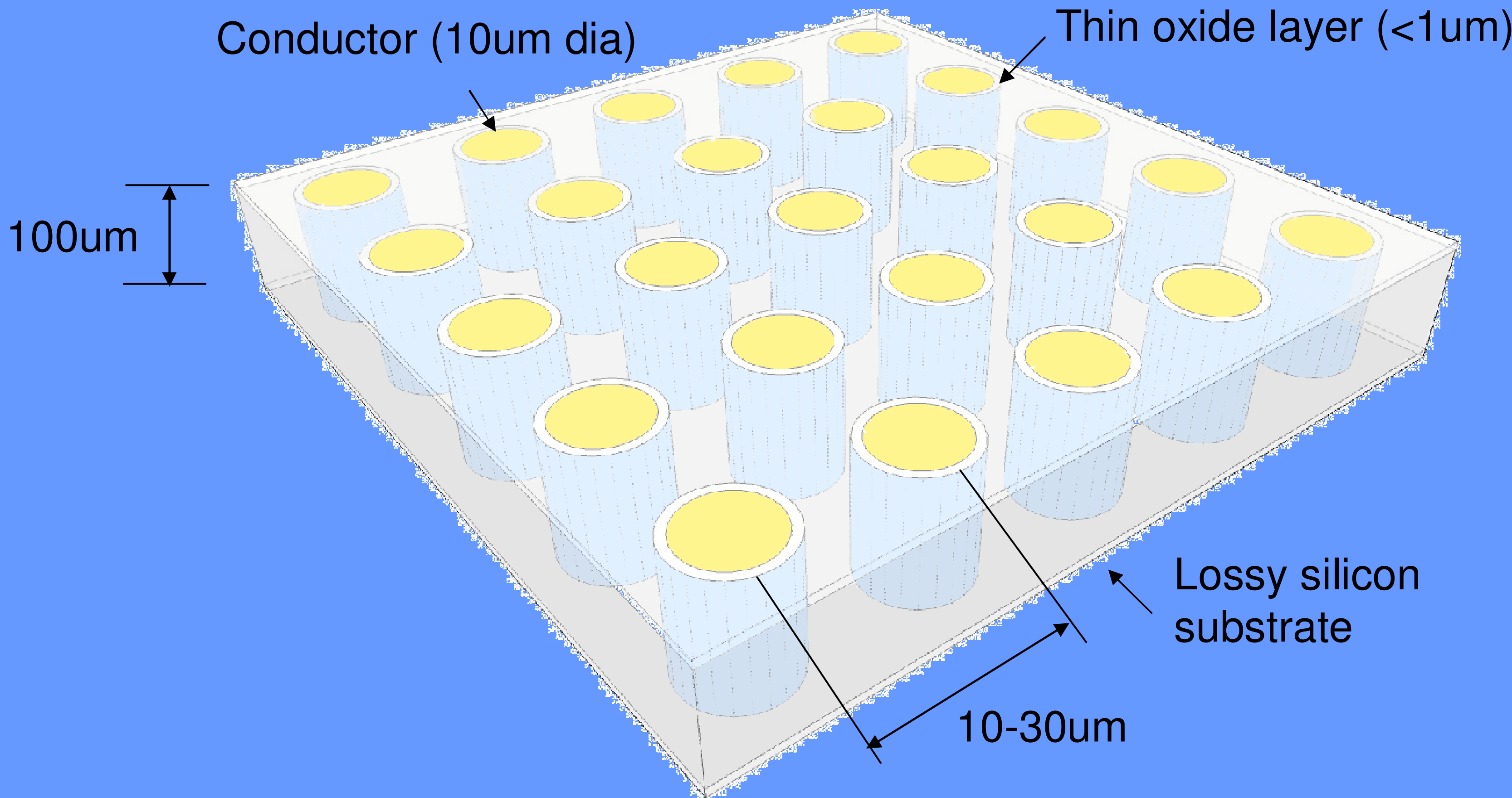


Joule Heating/Electro-migration



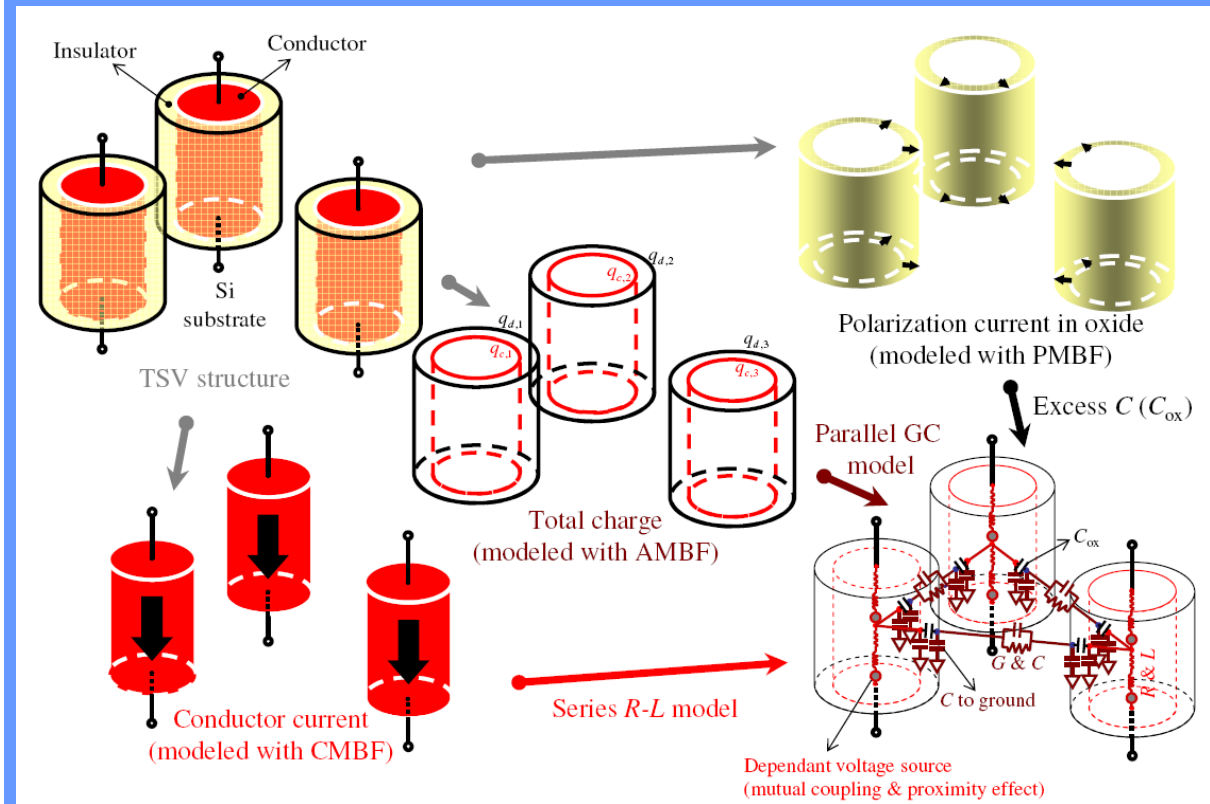
Thermal Management

Electromagnetic Modeling of TSVs
Multi-scale Challenge

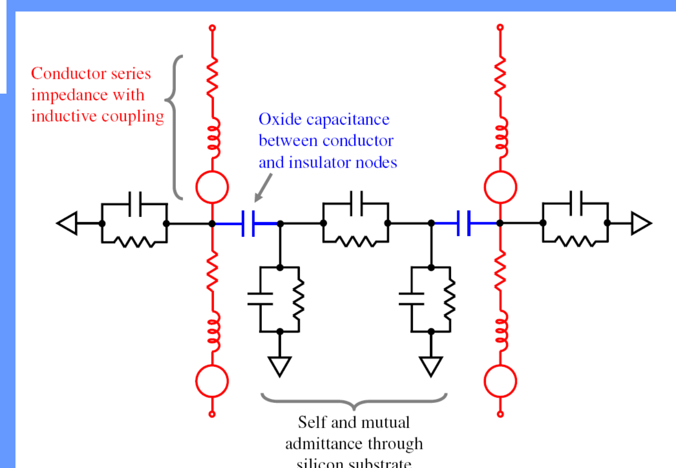


Commercial Tools will choke due to the multi-scale geometries of these structures

Modeling of TSVs using an Integral Equation Based Meshless Approach



- ❑ Uses Cylindrical Basis Functions – CMBF, AMBF, PMBF
- ❑ Solves Electric Field Integral Equation
- ❑ Uses Acceleration Methods



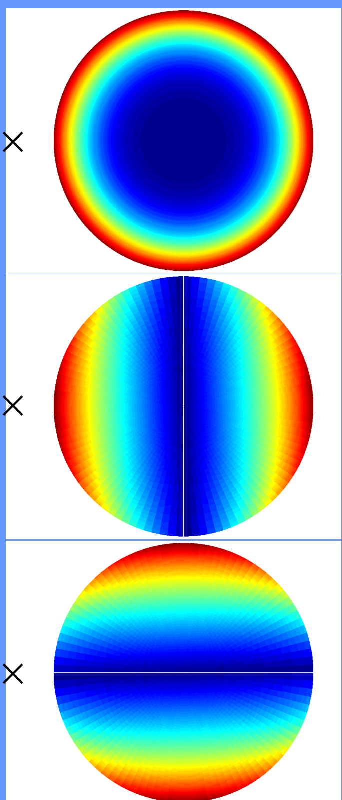
- ❑ Computes frequency dependent RLGC parameters
- ❑ Computes accurate coupling and loss occurring due to proximity effect
- ❑ Computes hot spots (current distribution)
- ❑ TSV position can be arbitrary

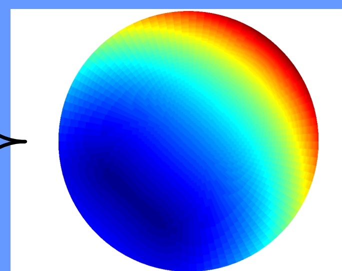
Using Modal Basis Functions to Extract Electromagnetic Properties of TSVs

1× SE mode

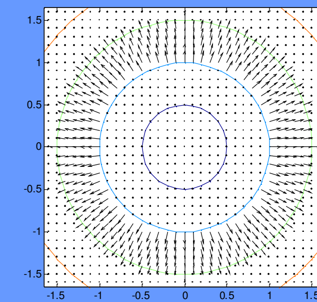
0.5× PE-*d* mode

0.5× PE-*q* mode

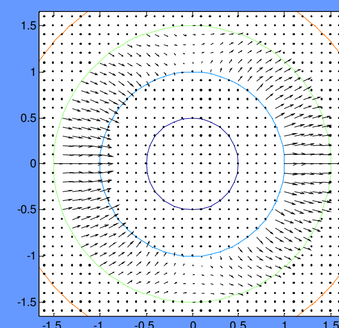




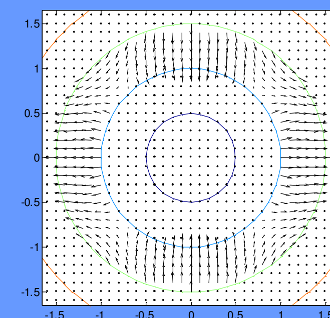
Resultant current density distribution



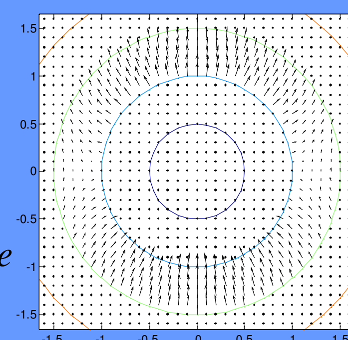
Fundamental

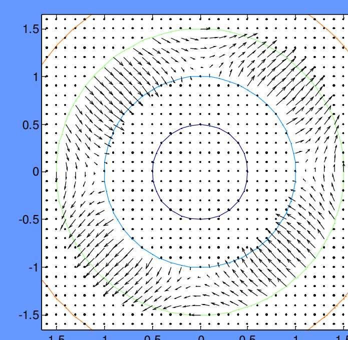


1st Mode



2nd Mode



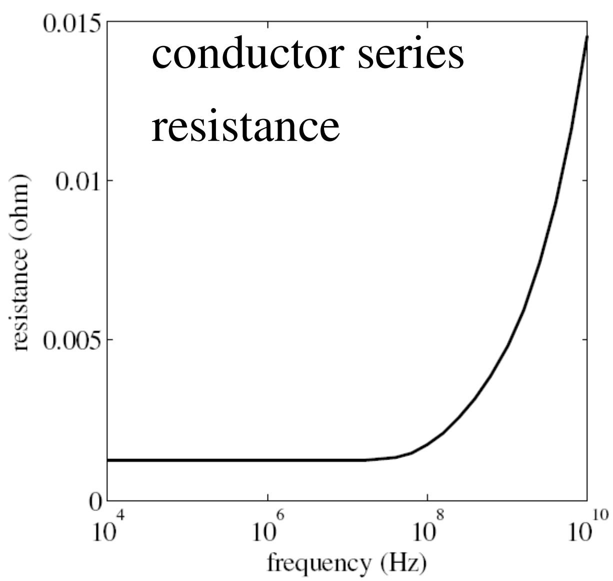


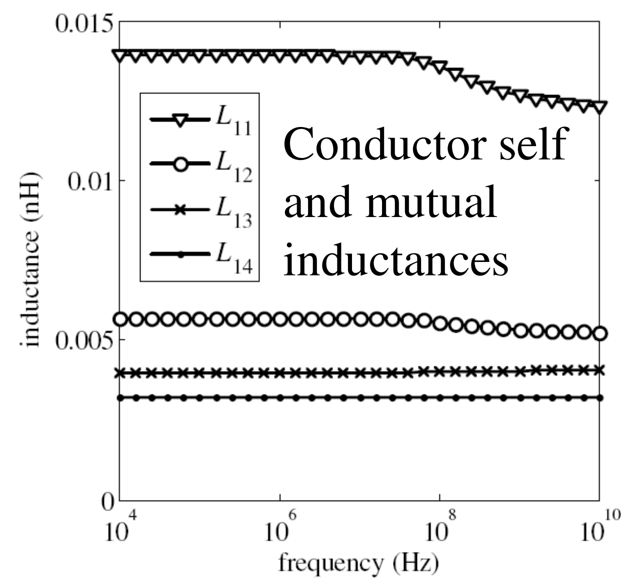
Polarization Effect Modes

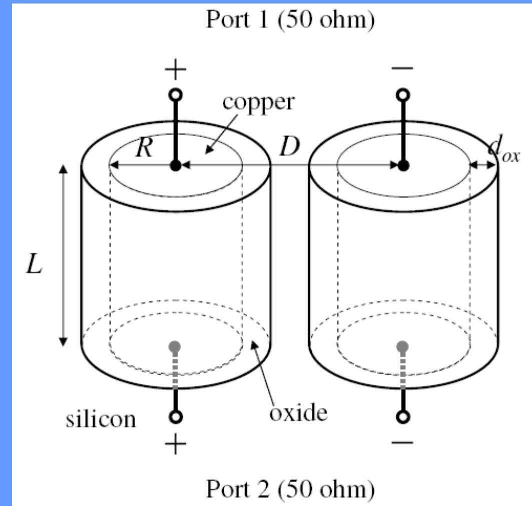
Skin and Proximity Effect Modes

Ref: K. J. Han and M. Swaminathan, "Inductance and Resistance Calculations in Three-Dimensional Packaging using Cylindrical Conduction Mode Basis Functions", IEEE Trans. on Computer Aided Design of Integrated Circuits & Systems, '09

TSV RLGC Parameter Extraction







TSV Structure

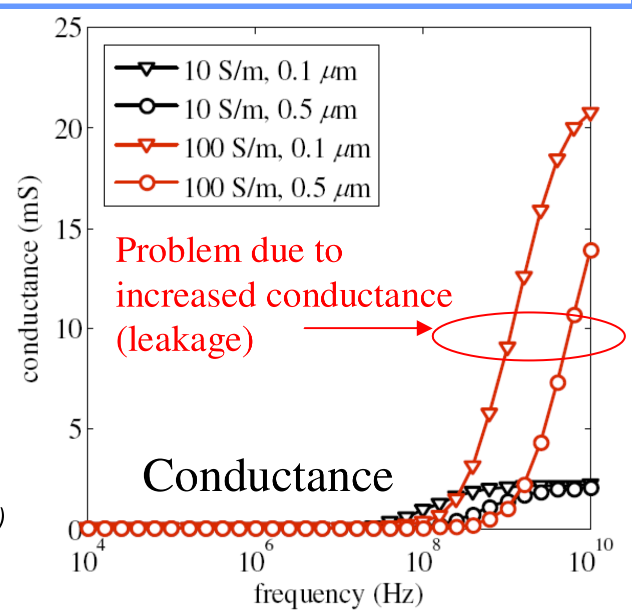
L=100um

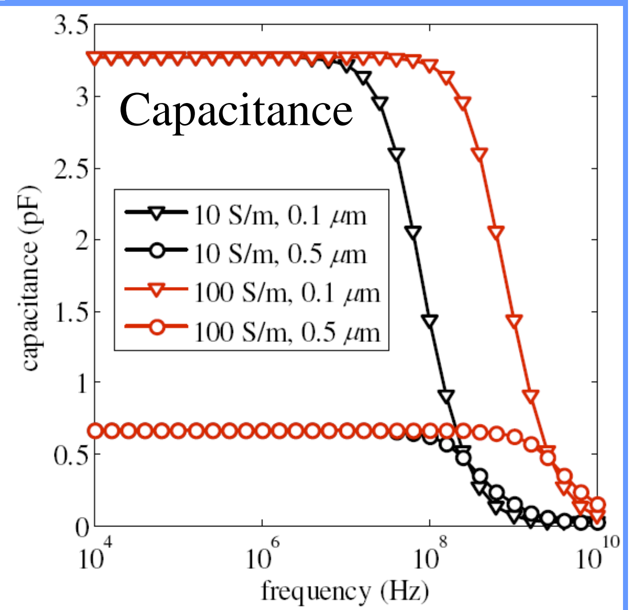
D=30um

P=60um

Grounded Substrate

K. J. Han, M. Swaminathan and T. Bandhyopadyay, " Electromagnetic Modeling of Through-Silicon Via (TSV) Interconnections using Cylindrical Modal Basis Functions", IEEE Trans. on Advanced Packaging, 2010

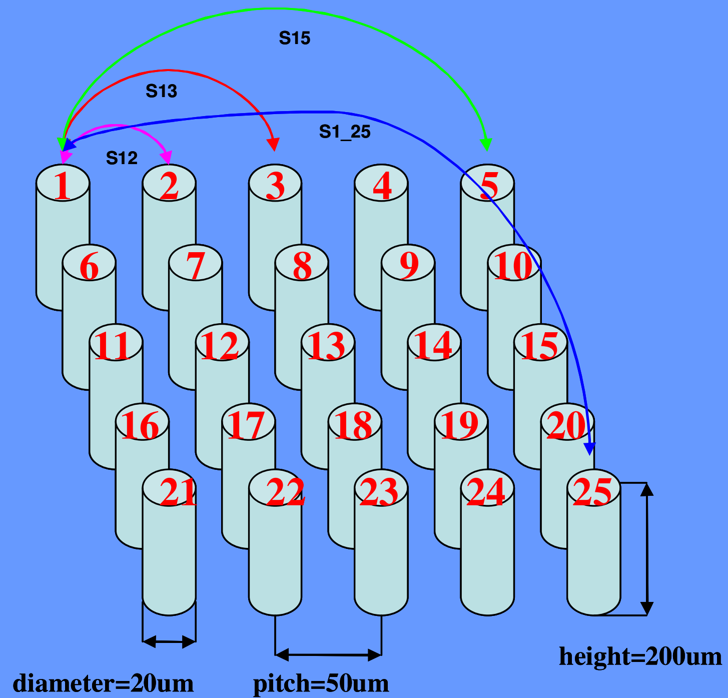




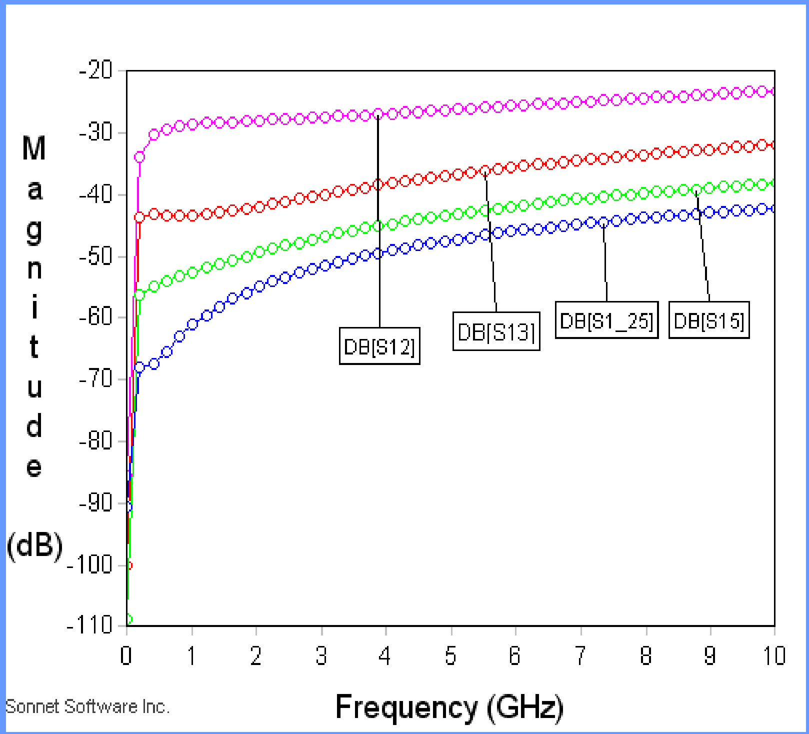
Coupling between TSVs – The Variability Problem

❑ ***TSV array Coupling***

- *5x5 TSV array*
- *Length: 200um*
- *Diameter:20um*
- *Pitch: 50um*
- *Oxide thickness: 0.1um*

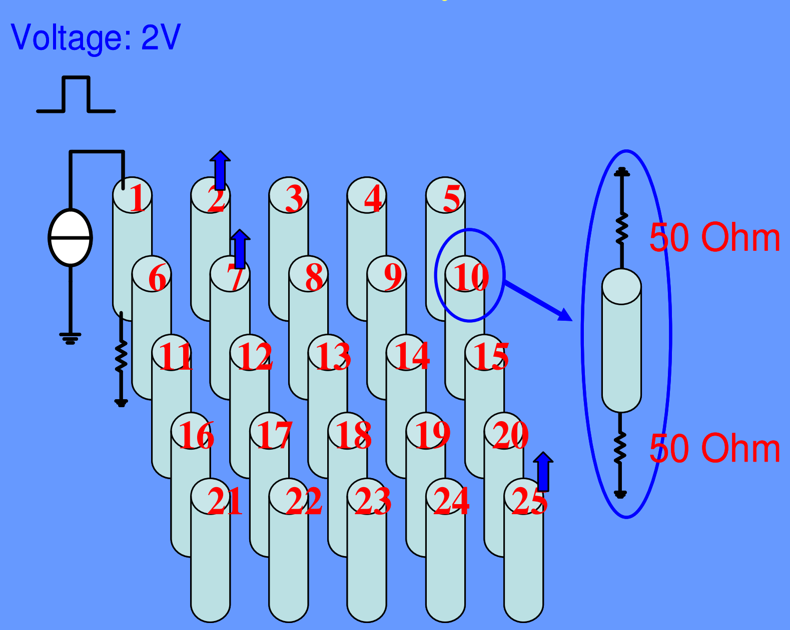


- ***Mutual Coupling between TSVs***
  - Mutual coupling reduced with increasing distance
  - But doesn't Vanish



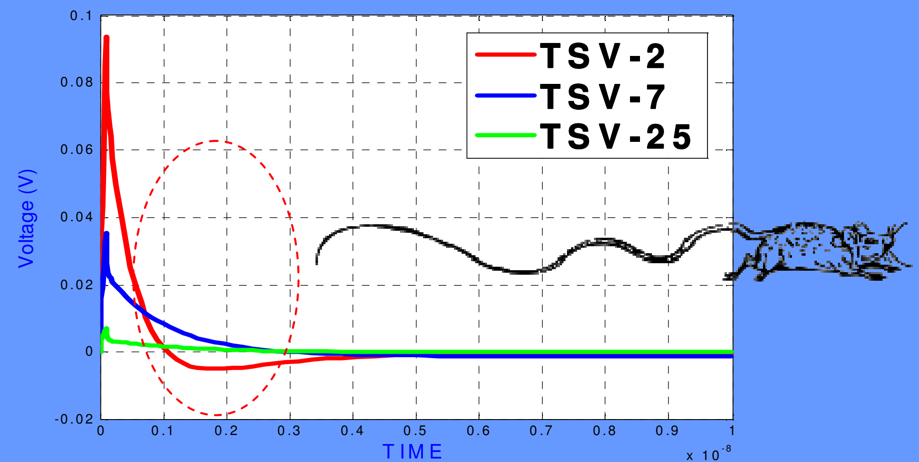
Crosstalk Waveforms – Low Vs High Resistivity Si

- ***Configuration***
  - A voltage pulse is applied at TSV-1
  - Pulse Rise and Fall time : 100ps
  - Substrate conductivity: 10 S/m or 0.01 S/m

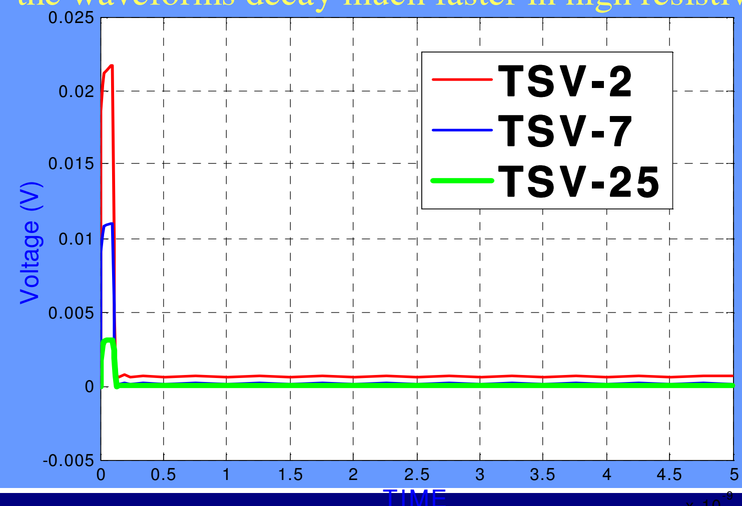


The Long Tail Problem ☹

- ***Coupling waveform at different TSVs (10S/m)***
  - the amplitude of the coupling waveform decrease with distance
  - the time constant of the waveform increase with distance

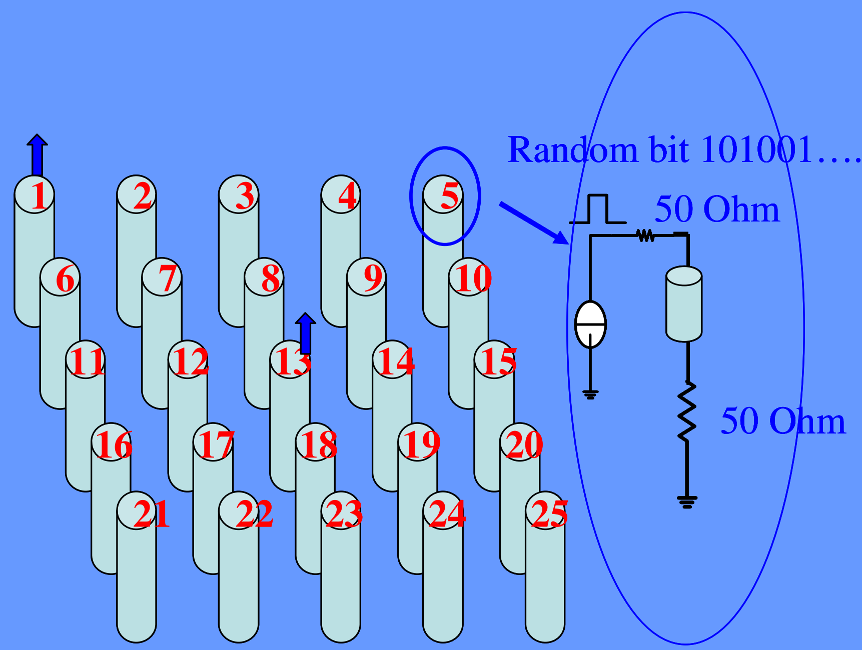


- ***Coupling waveform at different TSVs (0.01S/m)***
  - the amplitude of the coupling waveform decrease with distance
  - the waveforms decay much faster in high resistivity substrate

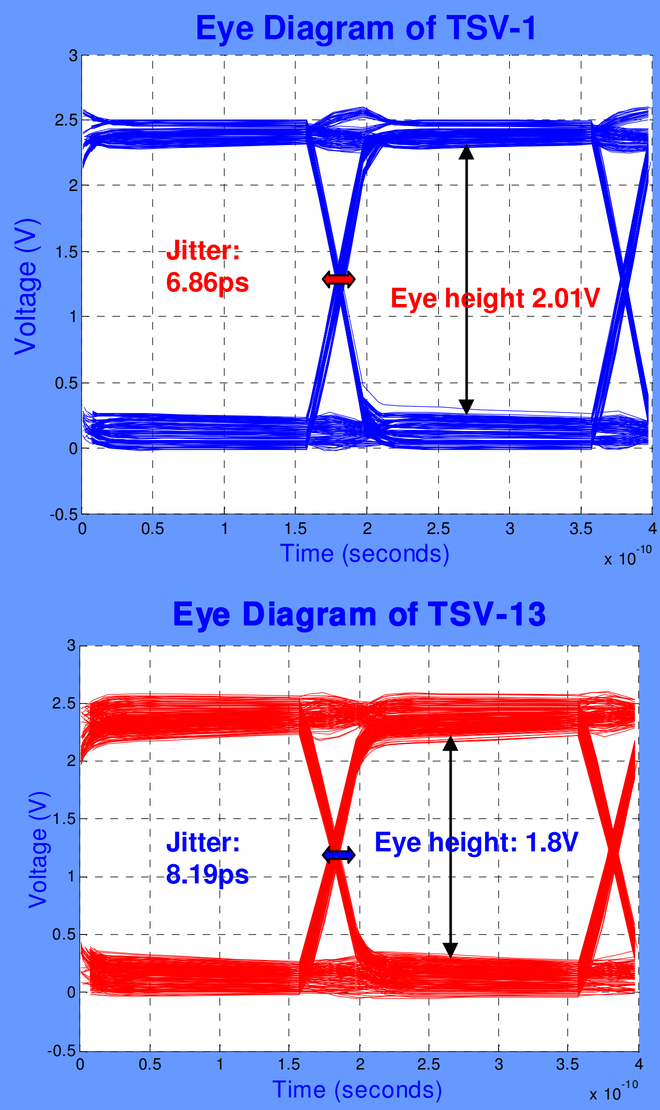


Variability in TSV Performance

- *Configuration*
  - Each TSV is connected with a Random bit generator
  - Bit sequences applied are different for each TSV
  - Bit rate: 5Gbps
  - Substrate conductivity: 10 S/m



All TSVs switching with a PRBS



Design of PDNs

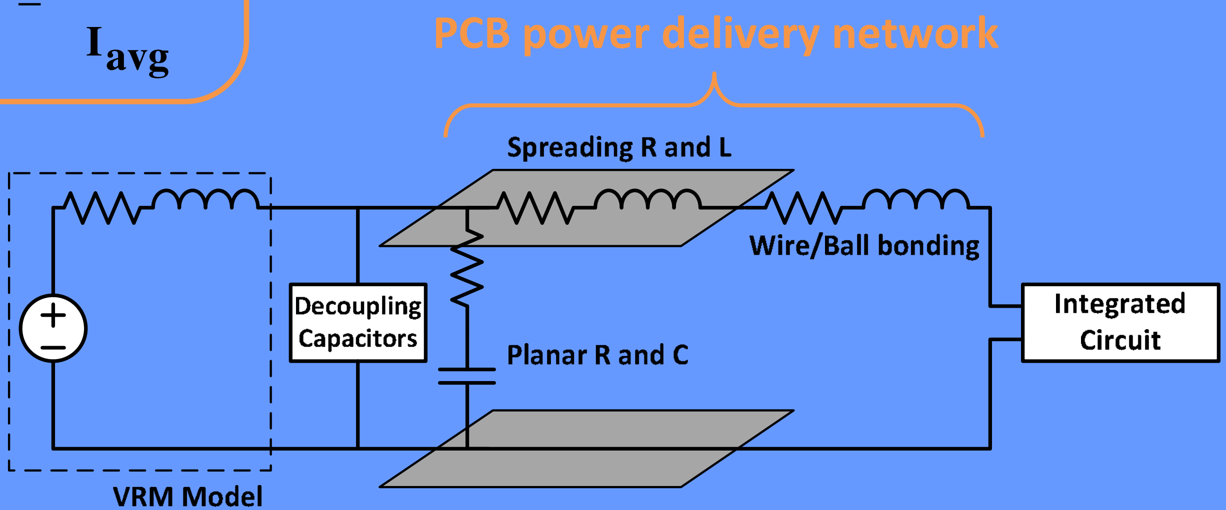
Currently Practiced design approach

Achieve a low-impedance path from the power supply to the die

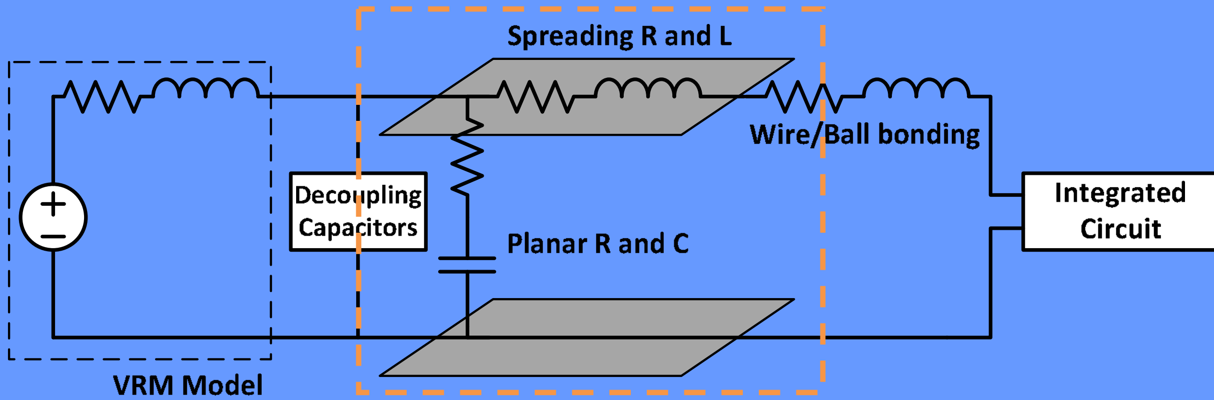
$$I_{avg} = \frac{P_{avg}}{V_{DD}}$$

$$Z_{target} = \frac{V_{ripple}}{I_{avg}}$$

→ $Z_{PDN} < Z_{target}$ → noise voltage < V_{ripple}



Two Sides of a Power Plane



Pros

- Provides low-impedance paths

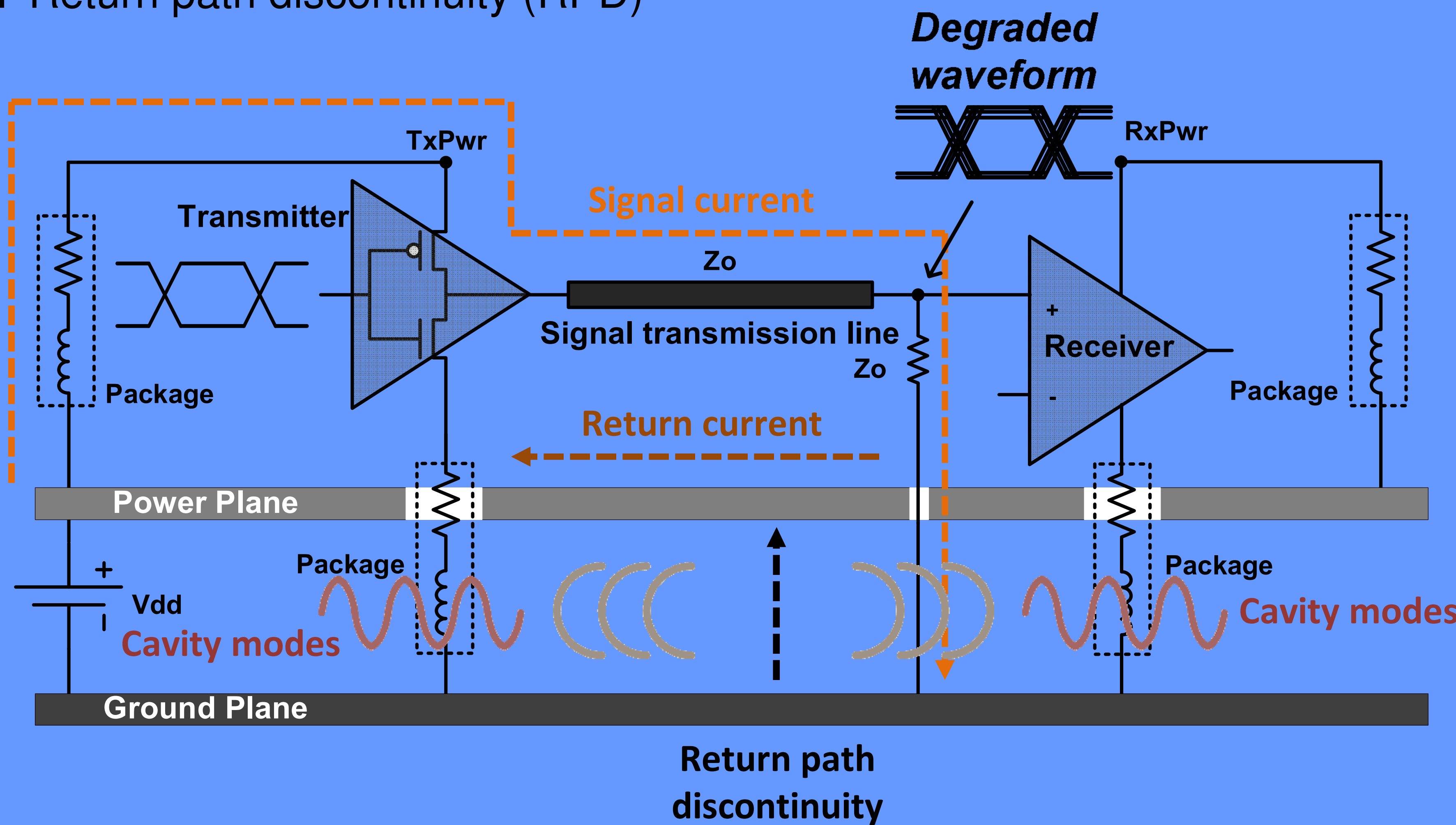
Cons

- Forms a cavity resonator
- Induces return path discontinuity
- Requires decoupling capacitors
- Needs computationally expensive design procedures

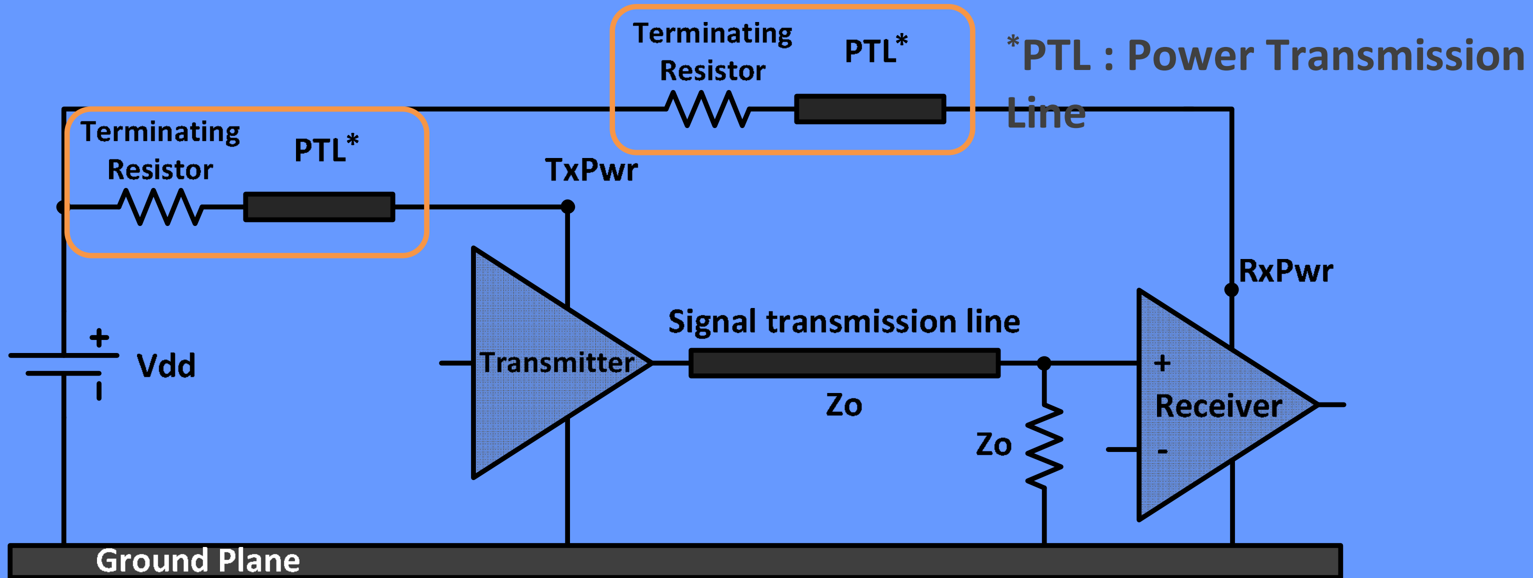
A new approach for PDN design is needed!

Conventional Power Delivery Network

- Return path discontinuity (RPD)



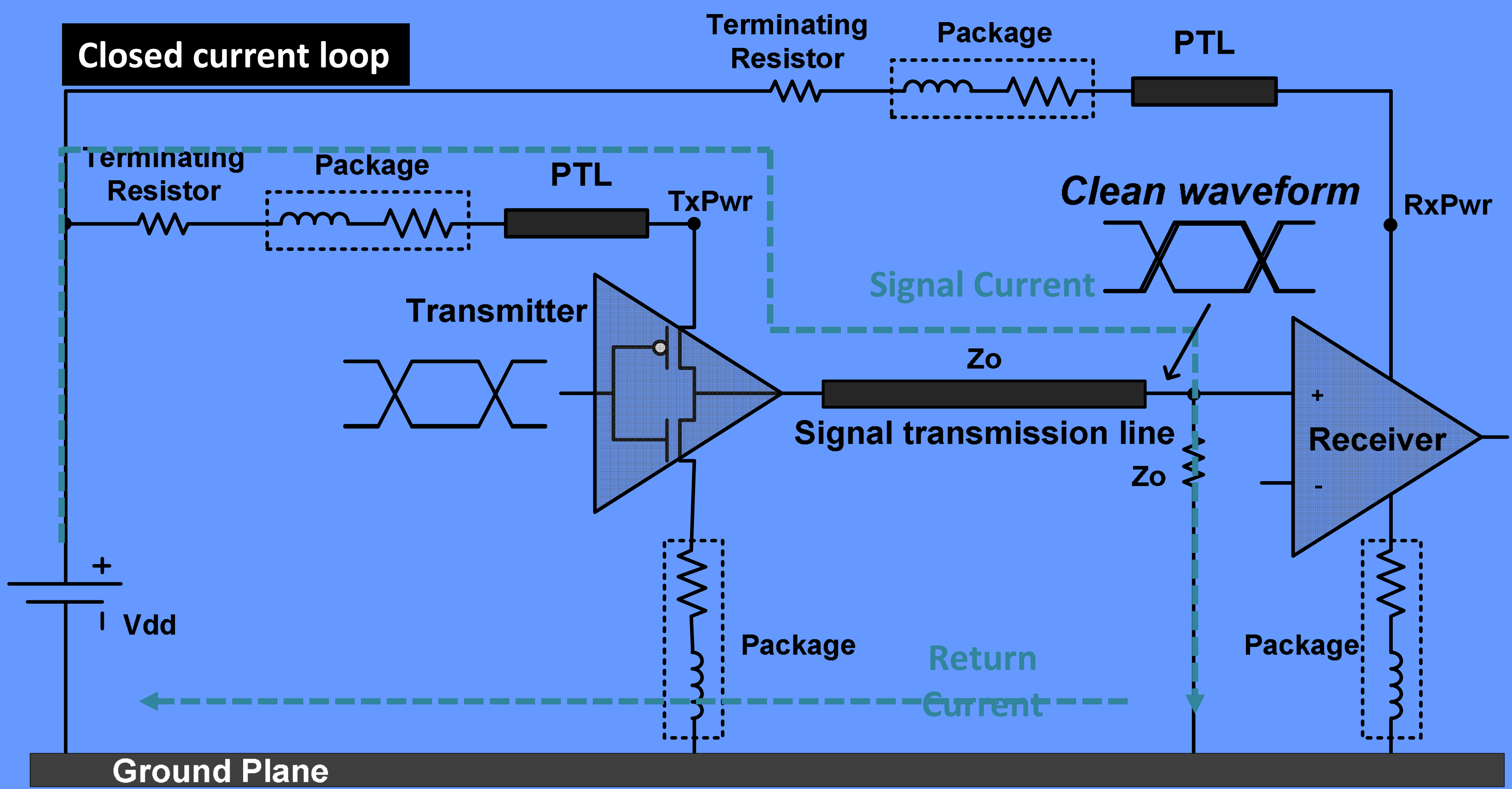
Power Transmission Line (1)



- ❑ Transmission lines replace the power plane to convey power
  - ➔ reduce the layer count
  - ➔ remove the effect of cavity mode resonance
- ❑ Both the power and signal transmission lines are referenced to the same ground plane
  - ➔ prevent the RPD (THIS IS A HIGH IMPEDANCE PDN)

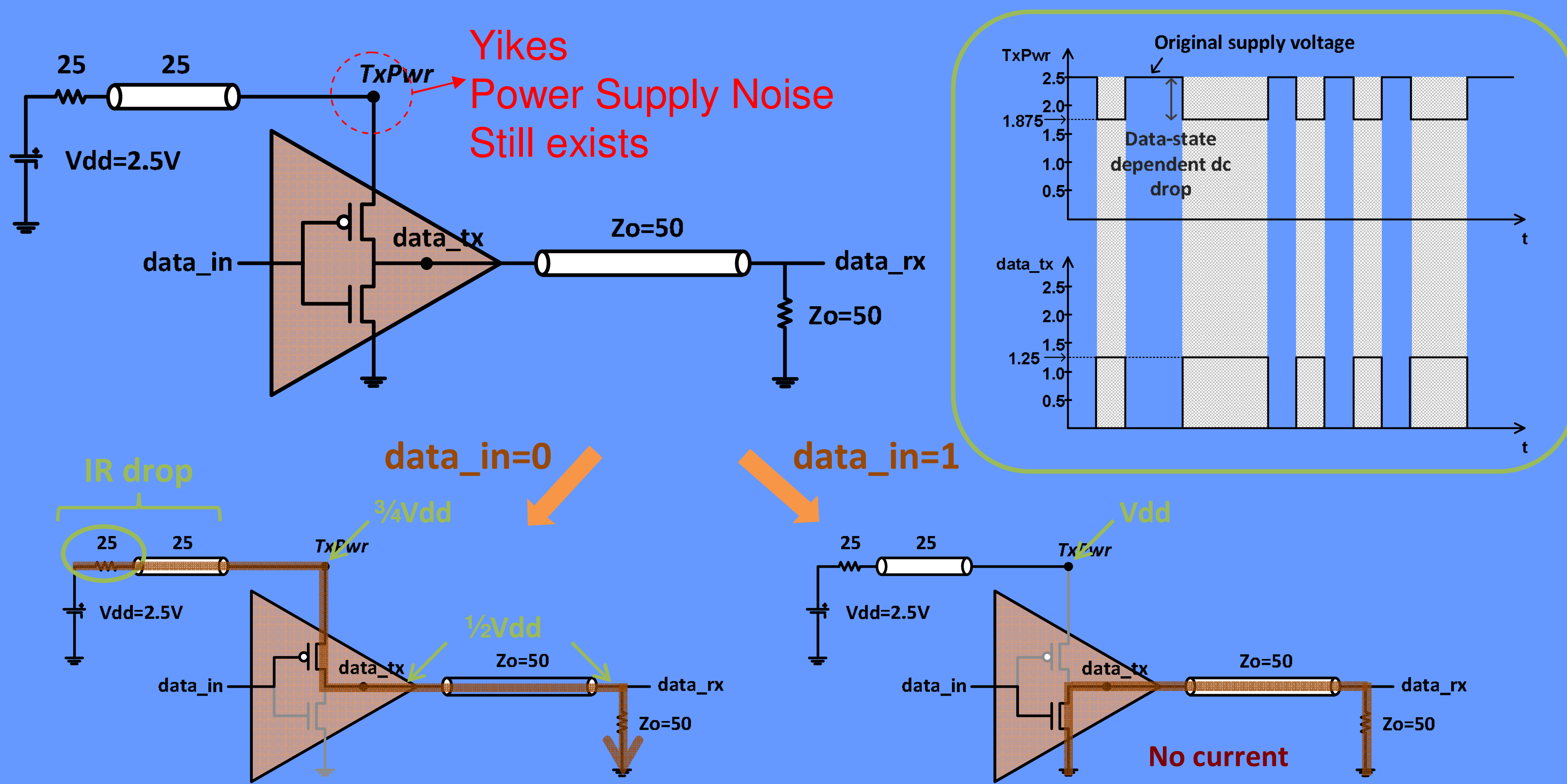
A. E. Engin and M. Swaminathan, "Power Transmission Lines: A New Interconnect Design to Eliminate Simultaneous Switching Noise," in Proc. ECTC, pp. 1139-1143, 2008

Power Transmission Line (2)



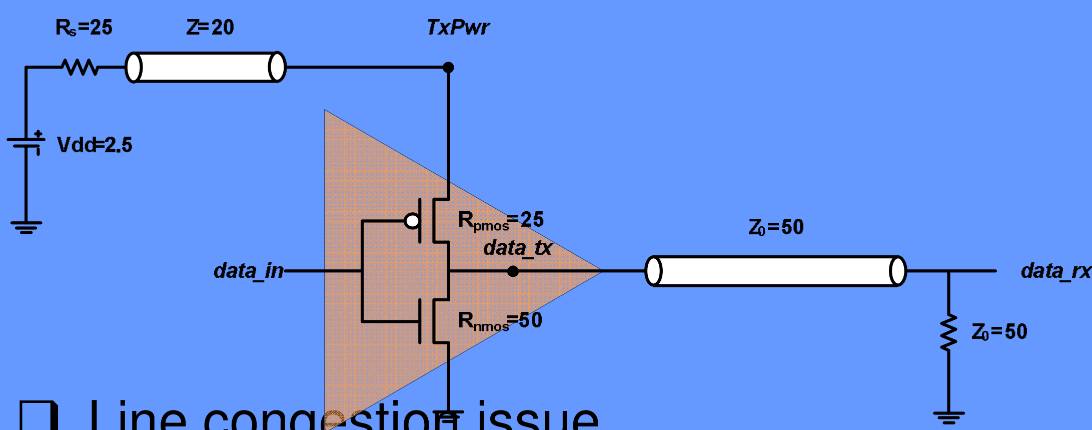
Limitation of Power Transmission Line(1)

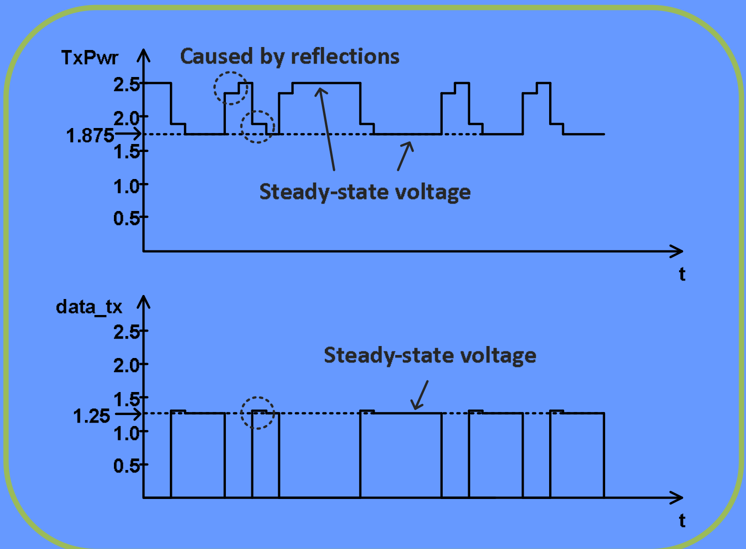
- DC drop on PDN due to DC resistance



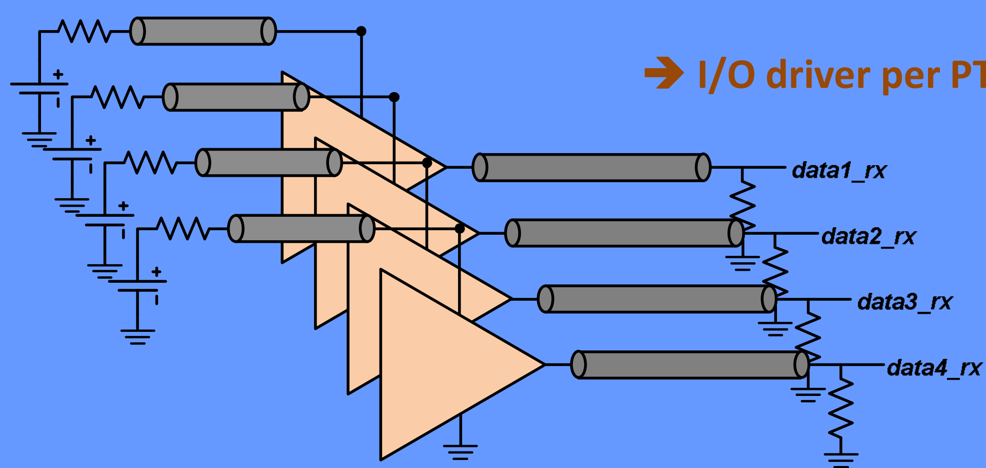
Limitation of Power Transmission Line(2)

- Impedance mismatch in PTL





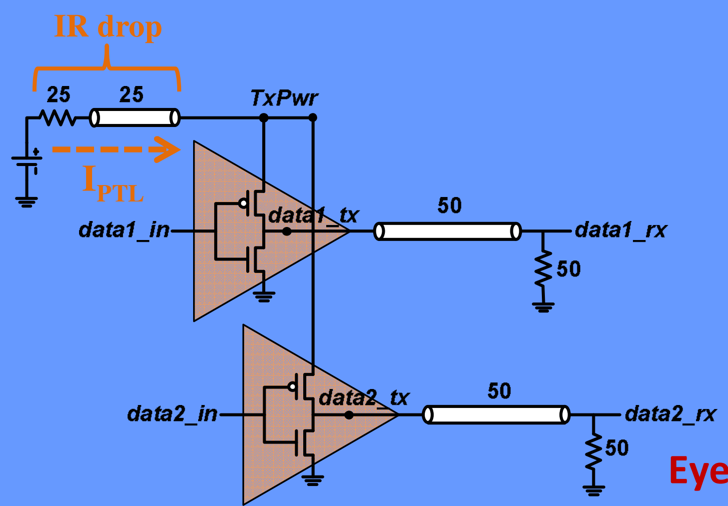
- Line congestion issue



➔ I/O driver per PTL will double the # of lines on PCB

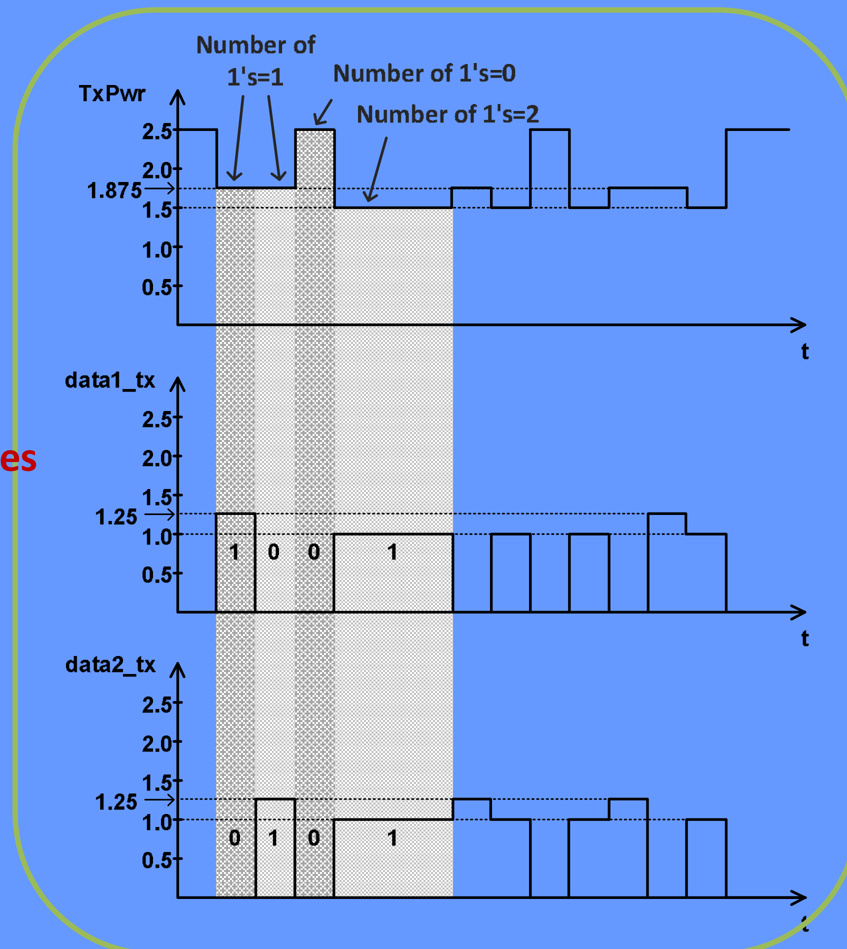
Limitation of Power Transmission Line (3)

- Varying DC Level on PDN when extended to multi-bit I/Os

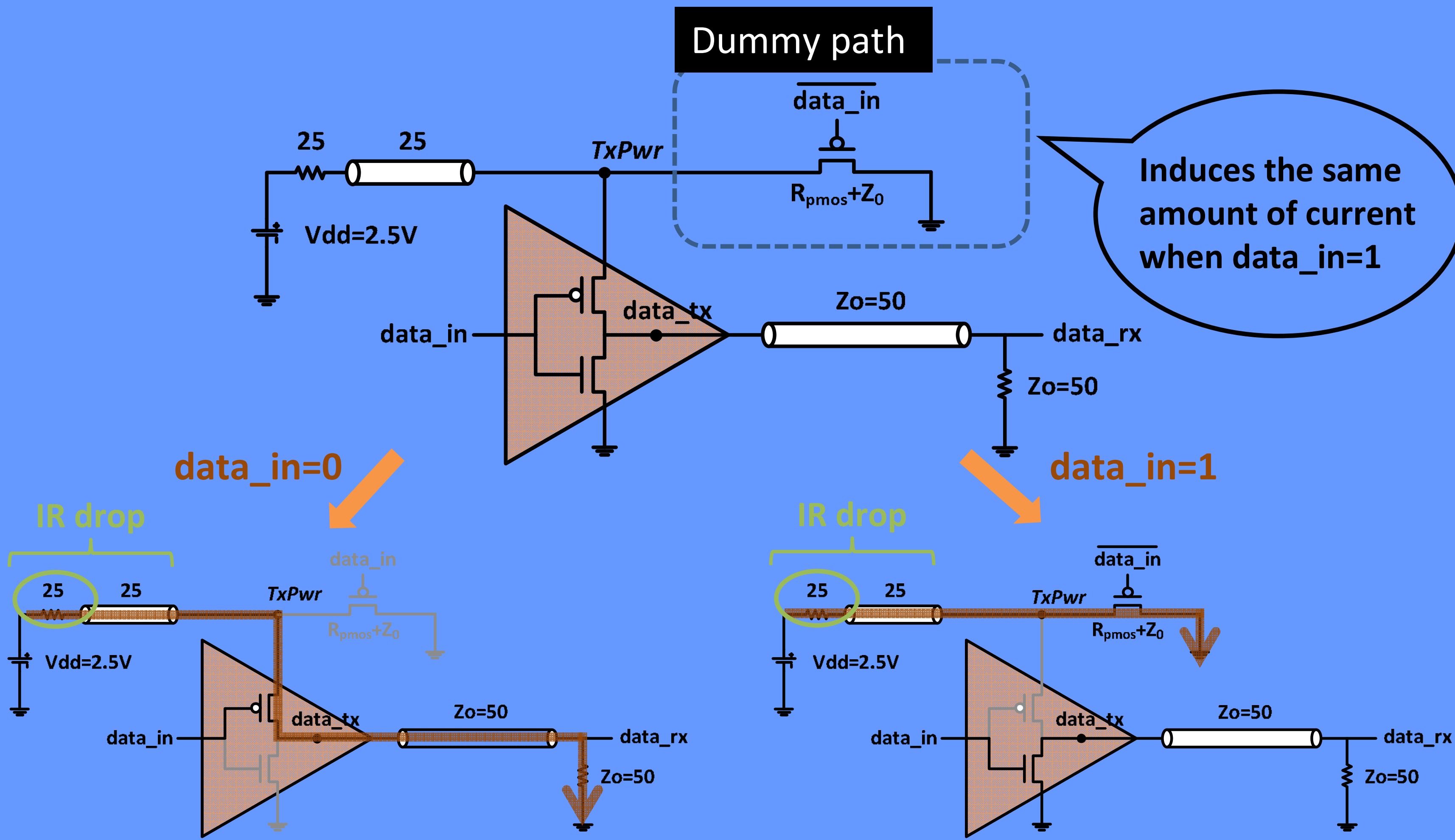


Eye height varies

Case	Data Pattern		Eye Height	
	data1_tx	data2_tx	data1_tx	data2_tx
1	High	High	1V	1V
2	High	Low	1.25V	0
	Low	High	0	1.25V
3	Low	Low	0	0

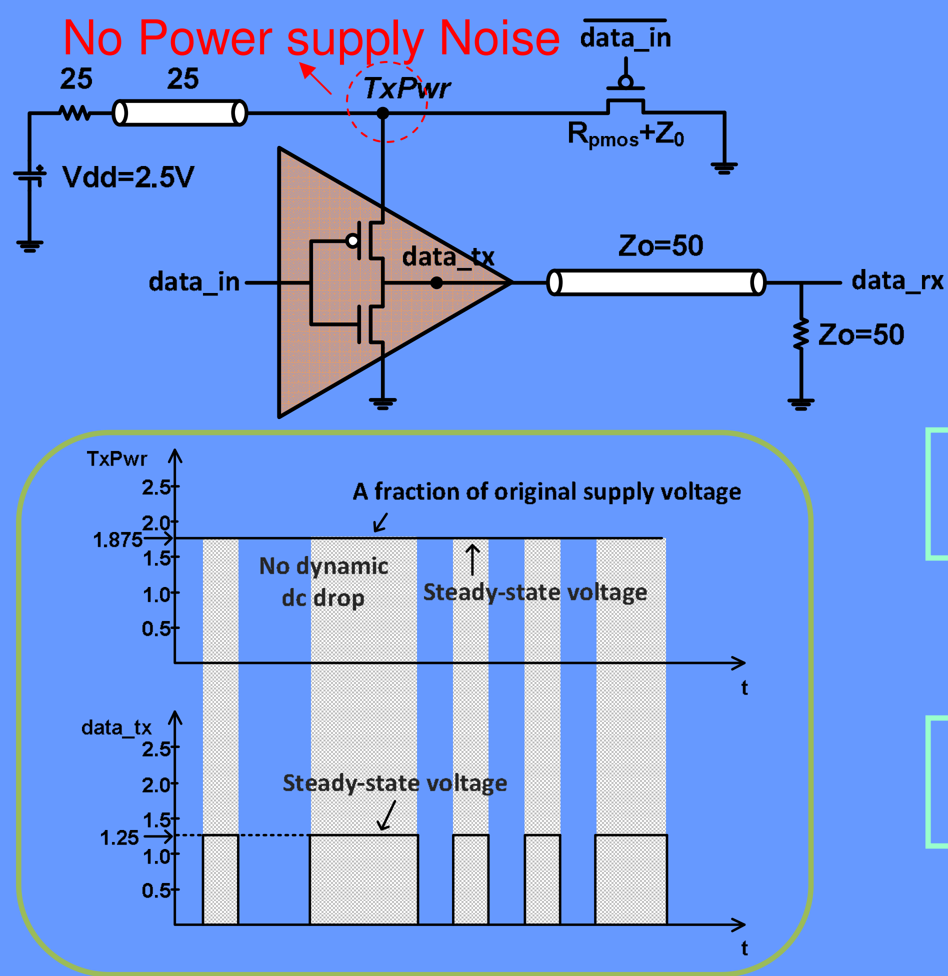


Constant Current PTL (1)



Constant Current PTL (2)

- Constant current power transmission line (CC-PTL)



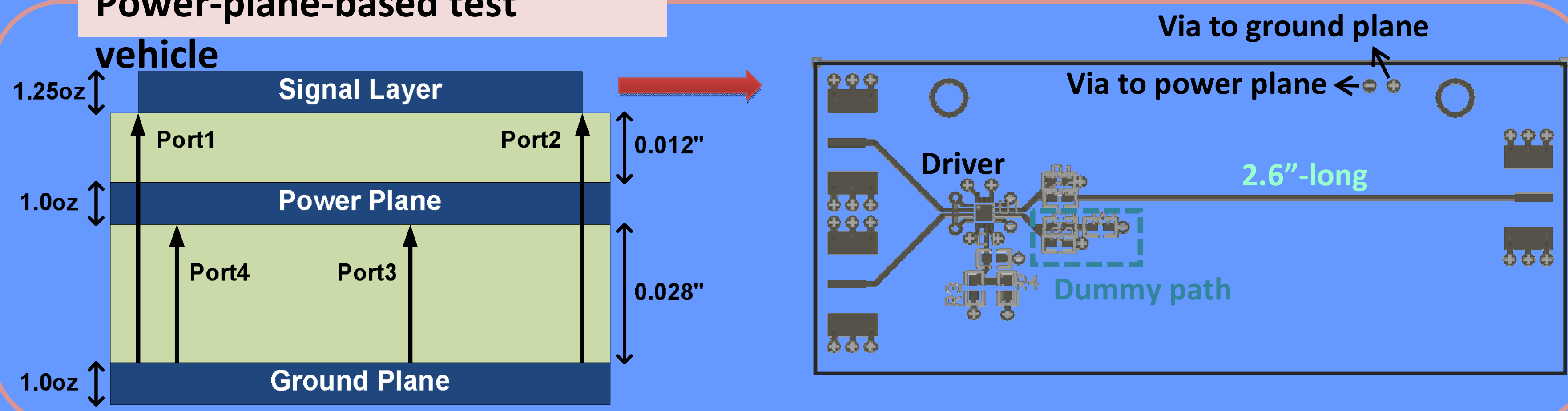
Constant current through PTL

Constant IR drop over PTL → Constant voltage at TxPwr node

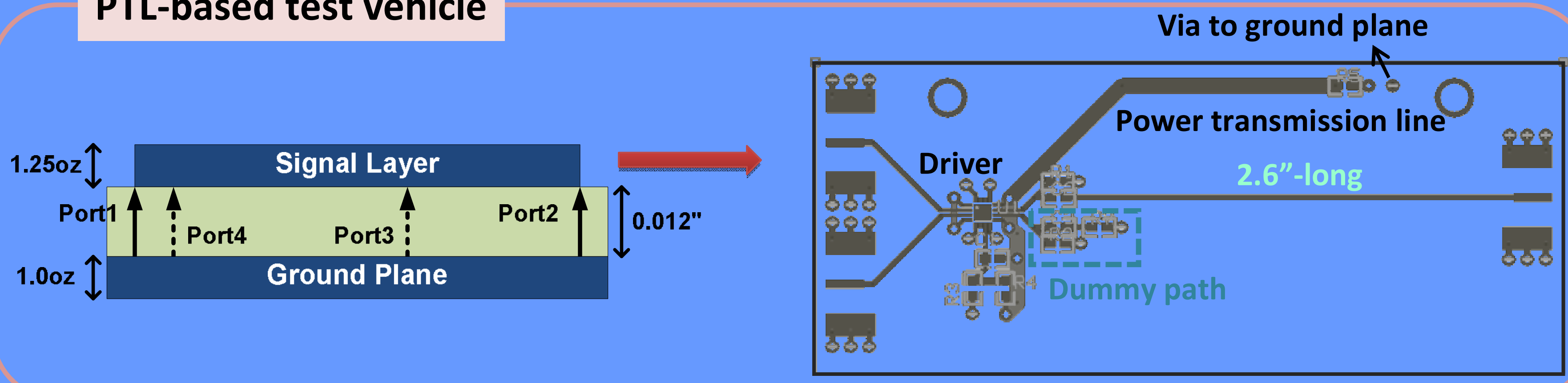
Continuously charged PTL → No mismatch effect

Test Vehicles

Power-plane-based test vehicle

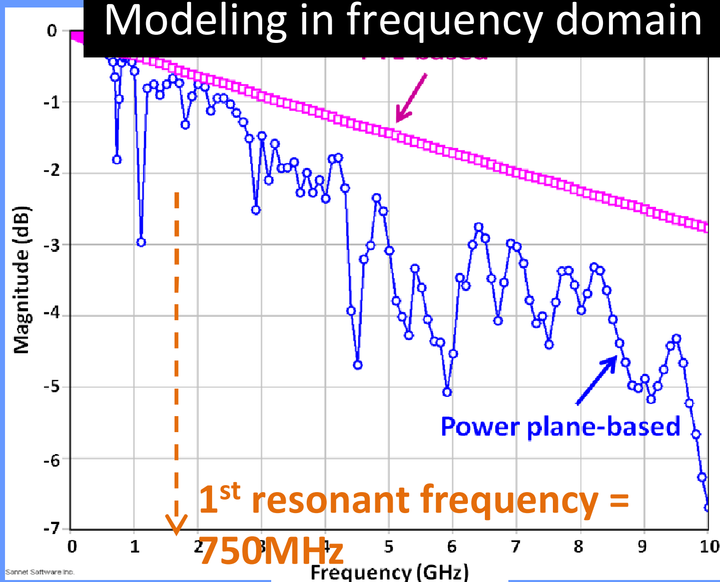


PTL-based test vehicle



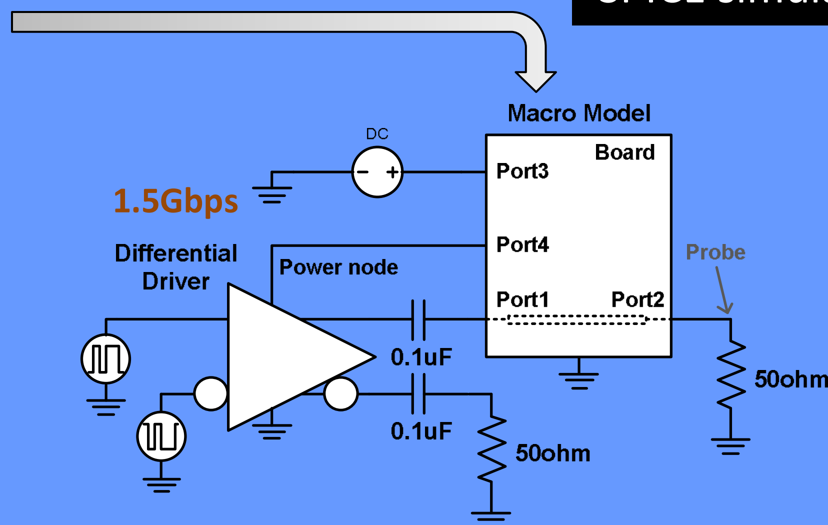
Modeling and Simulation

Modeling in frequency domain

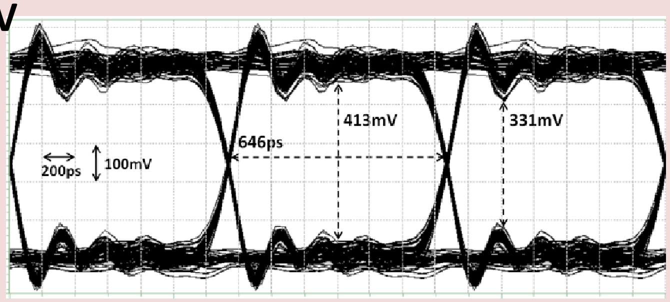


Converted to Macromodel

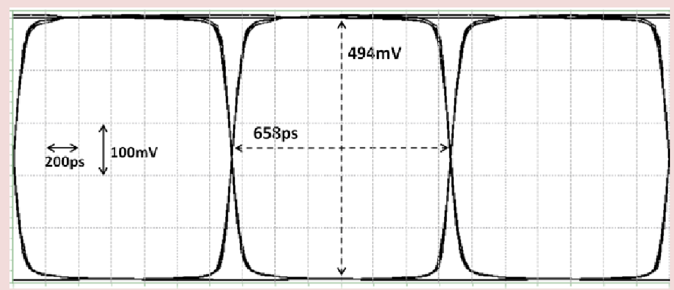
SPICE simulation setup



Power-plane-based TV

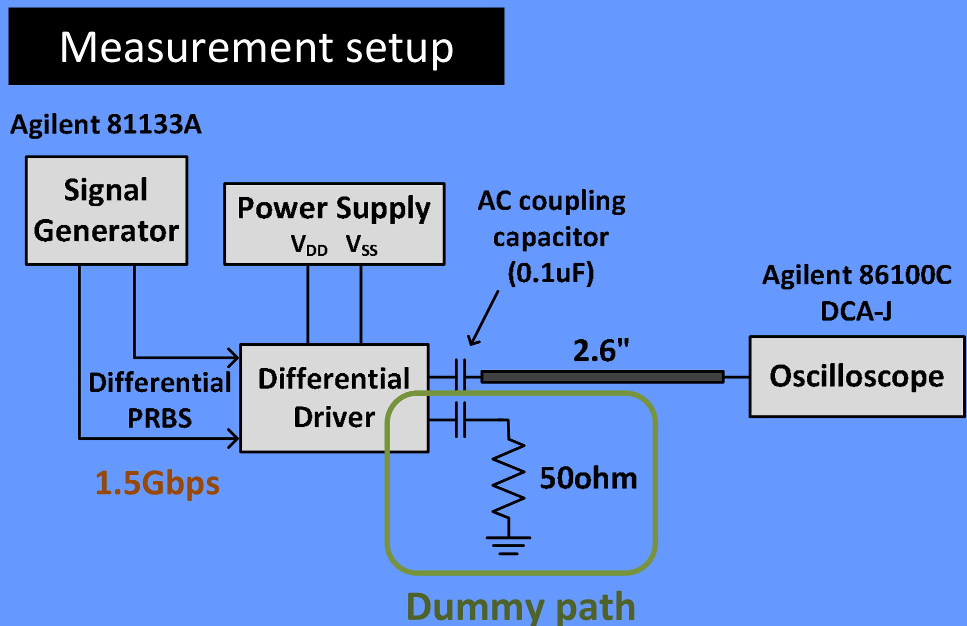


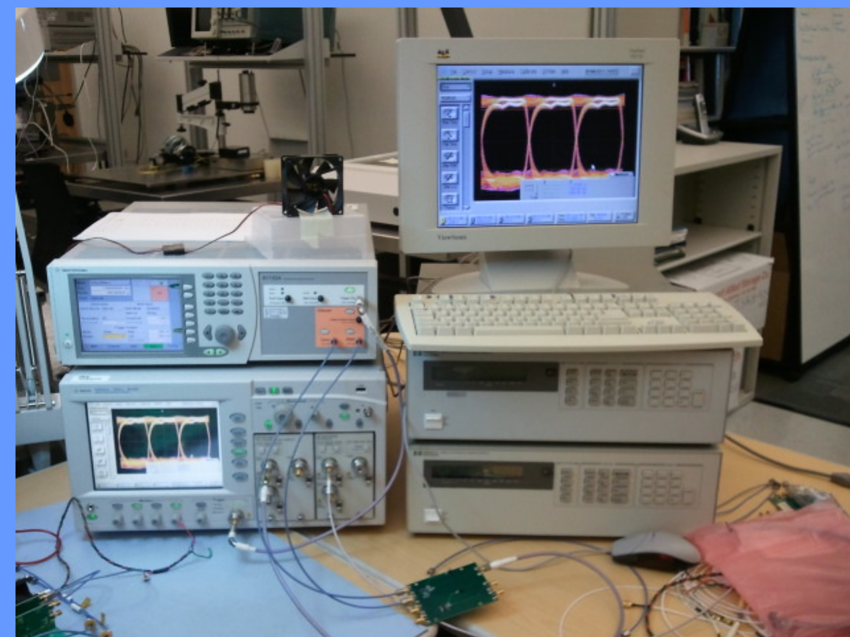
PTL-based TV



Eye height improves by 19.6%
Jitter improves by 58%

Measurement Setup

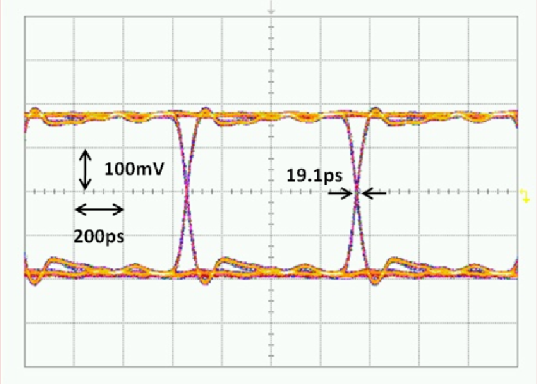




- The dummy path is implemented outside the chip due to the limitation of using an off-the-shelf chip
- AC coupling capacitor is used
  - to suppress the DC current flow
  - to provide bias for the oscilloscope

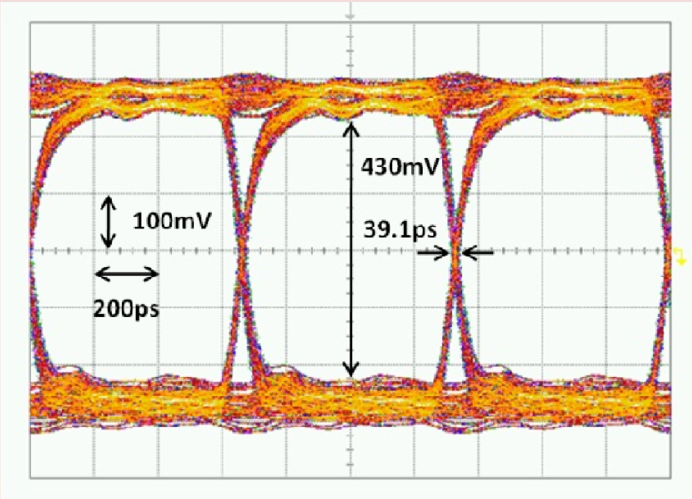
With Source Termination

Signal generator output

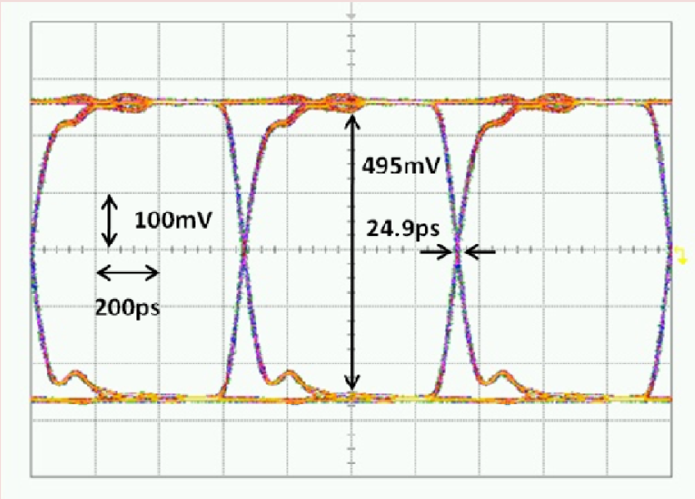


	Eye height	P-P jitter
Power plane	430mV	39.1ps
CCPTL	495mV	24.9ps
Improvement	15.1%	36.3%

Plane-based TV



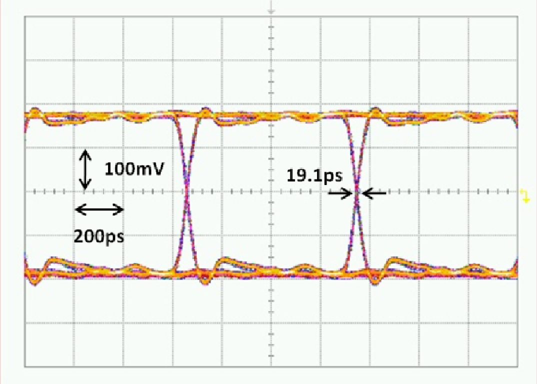
CCPTL-based TV



- **The supply voltage of 2.5V is used for the plane-based TV, while 3.47V is used for the PTL-based TV.**

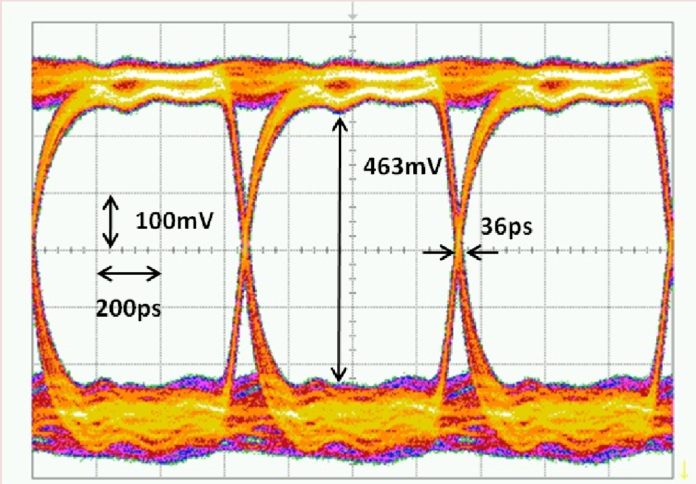
Without Source Termination

Signal generator output

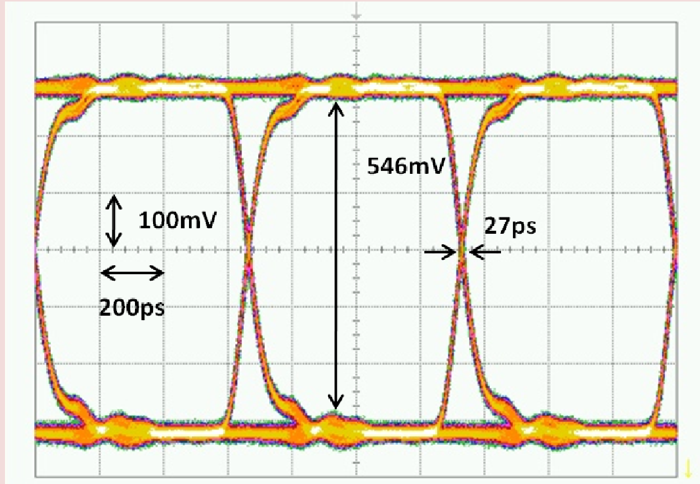


	Eye height	P-P jitter
Power plane	463mV	36ps
CCPTL	546mV	27ps
Improvement	17.9%	25%

Plane-based TV

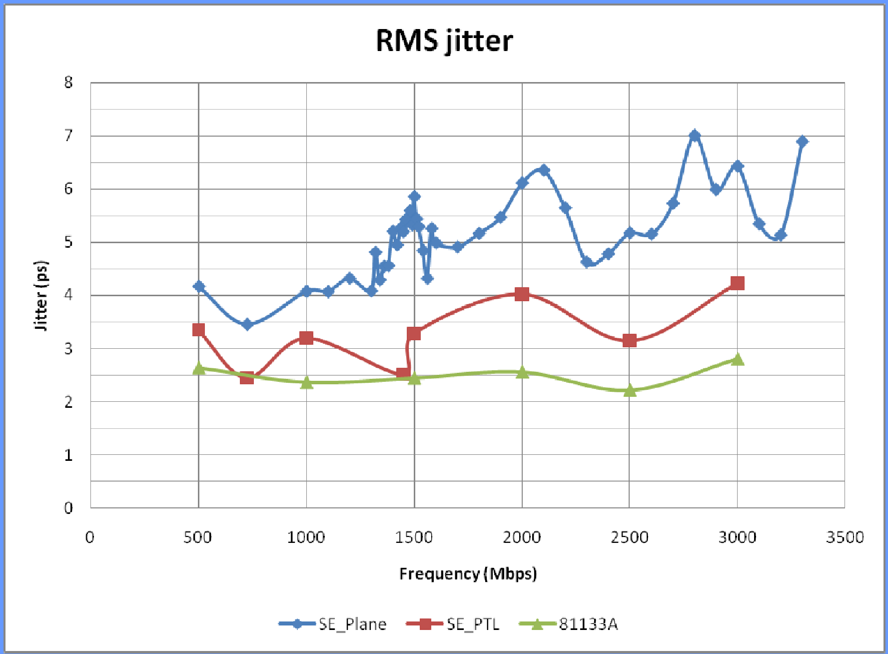


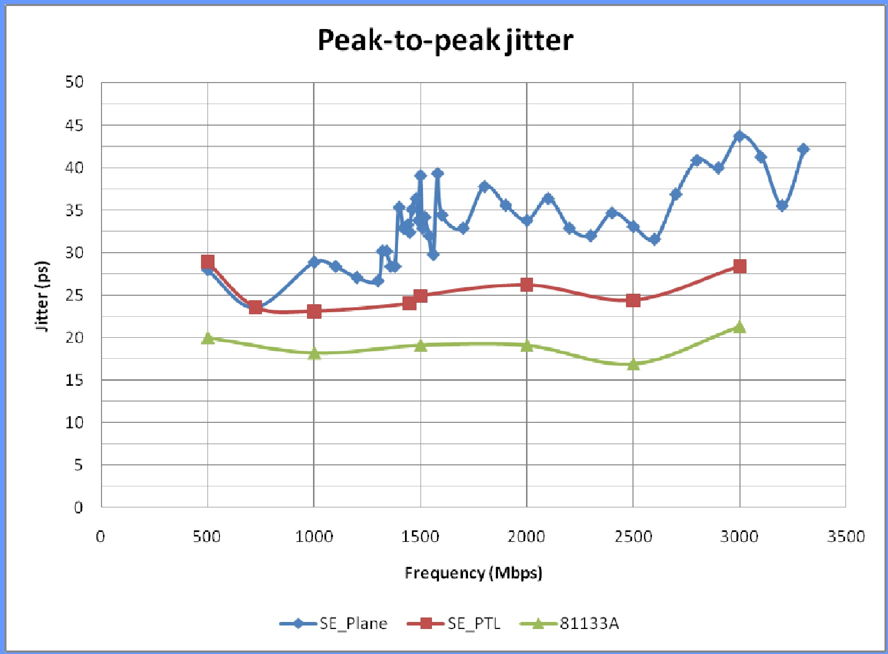
CCPTL-based TV



- **The same supply voltage of 2.5V is used for both test vehicles.**
- **Mismatch between the signal line and load termination is negligible so that the source termination could be omitted.**

RMS and P-P Jitter Comparison





- ❑ PTL: Both RMS and P-P Jitters have relatively monotonic behavior.
- ❑ Power plane: Both RMS and P-P Jitters have non-monotonic behavior, having local peak values at the frequencies of power/ground plane resonances.

Summary for Power Transmission Line

- **The first demonstration of the CCPTL scheme has been presented – A High Impedance PDN based concept**
- **Reduces decoupling capacitors required (not shown)**
- **Simulations are done to model the test vehicle in both frequency and time domains.**
- **Based on measurements, using the CCPTL scheme**
  - improves the eye height by 15.1% and p-p jitter by 36.3% with source termination
  - improves the eye height by 17.9% and p-p jitter by 25% with source termination
- The power consumption issue needs to be addressed
- This is being addressed through Constant Voltage Power Transmission Line concept – ongoing work

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