Use of Fast Digital Interfaces on Satellites and their relationship with EMC aspects

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- Conclusions.

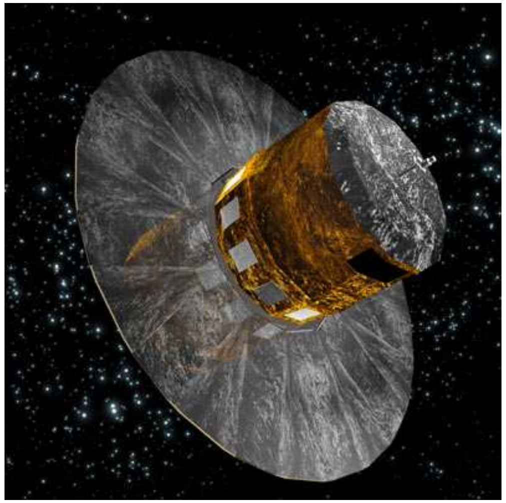
Present and future scenario

The current and the next future scenario of the scientific satellites is characterized by an increasing design complexity in term of amount of mass memory, data throughput and on-board processing capabilities.

Central Processing Units running at hundred of Megahertz are used as central core of Payload Computers and their high performance is able to acquire data coming from large detectors, process and transmit huge amount of data towards Flight Mass Memory Units for a temporary storage and finally to Earth.

ESA IMAGE

James Webb Space Telescope



ESA IMAGE

Gaia

Present and future scenario

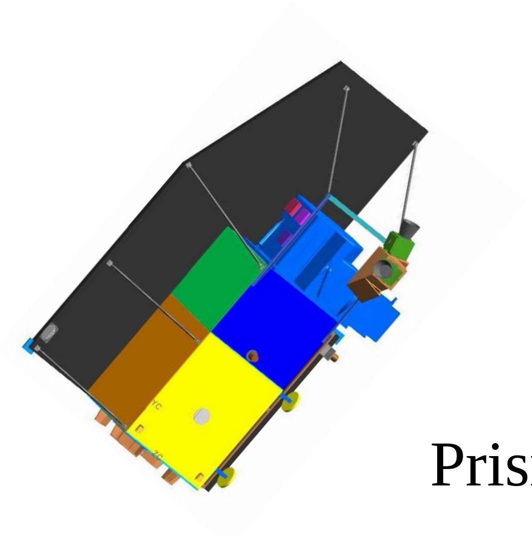
Mass Memory: the GAIA satellite will have a mass memory unit of 800Gbits, the Sentinel 1-3 satellites a capacity of 1.6-2 Tbits. The italian PRISMA satellite will have a memory size of 256-512Gbits. All the sizes are to be considered EOL (End of Life).

The mass memory units are and will be based on the commercial SDRAM II and III technology with a data throughput up to 1-6Gbps.

The currently required performance of the MMU has to be compared with a capacity of < 1Gbit of the space Hubble telescope (1990, with a data throughput less than 20Mbps) or the 4Gbit of Rosetta MMU (launched in 2003) with a data throughput of 100Mbps appx.

ESA IMAGE

Bepi Colombo



Prisma (ASI)

Present and future scenario

Beside the standard functions of MMU (like reception of raw and/or formatted data from the P/L-instruments via multiple input channels, data storage and retrieval function including data protection against generic and/or radiation induced data failures , downlink data into CCSDS or other formats, …) new optional functions are required:

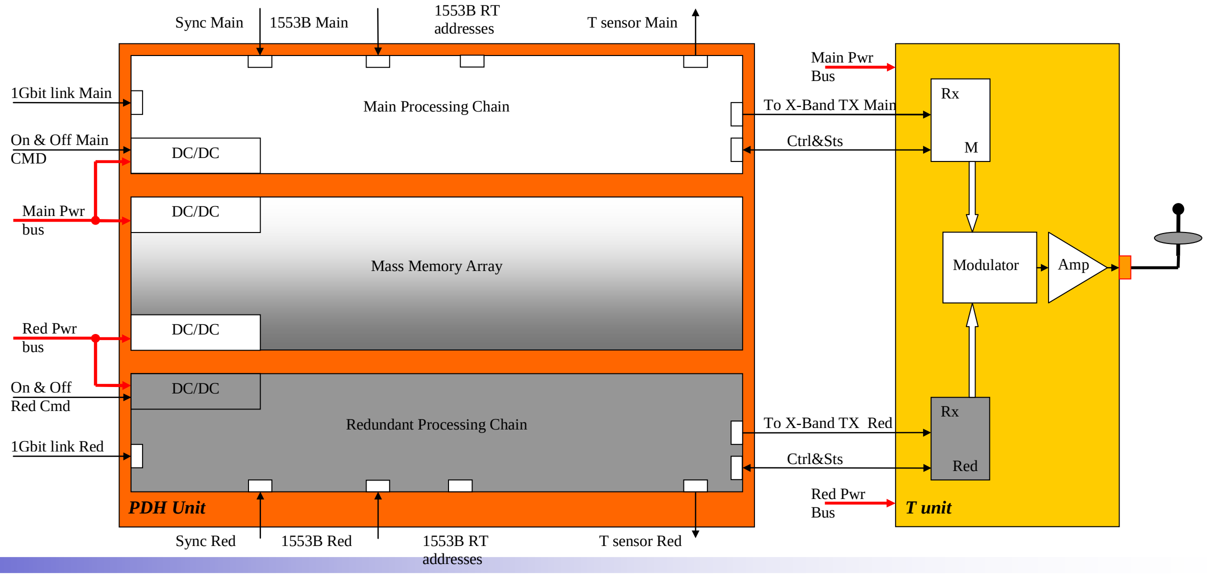
- Data compression
- Data encryption

Why an increase of the size of the mass memory units? Two reasons:

➢Bigger detectors/instruments that produce bigger amount of data

➢Limited visibility from Ground Stations

Power and Mass:Memory with a capacity of 1Tbits have a mass of 20-30kg with a power dissipation of 30-50W.



Present and future scenario

PROCESSORS USED in SPACE PROGRAMS (ESA, ASI) as CENTRAL CORE FOR PAYLOAD COMPUTERS:

Past and present scenario:

- 80c186 from Intel ,T800-805 from Inmos
- **TSC21020F/**DSP21020 from Atmel (60MFlops as peak performance, 40 MFLOPS as sustained performance, 20MIPS, Harvard architecture, 32-bit Single-Precision and 40-bit Extended-Precision IEEE Floating-Point Data Formats, 20 MHz as Maximum clock frequency),
- **TS695F**/ERC 32 GPP (Sparc V7 Risc Unit, 20 MIPs/5 MFlops (Double Precision) at SYSCLK = 25 MHz, EDAC on board, 0.5um silicon lithography process by Atmel),

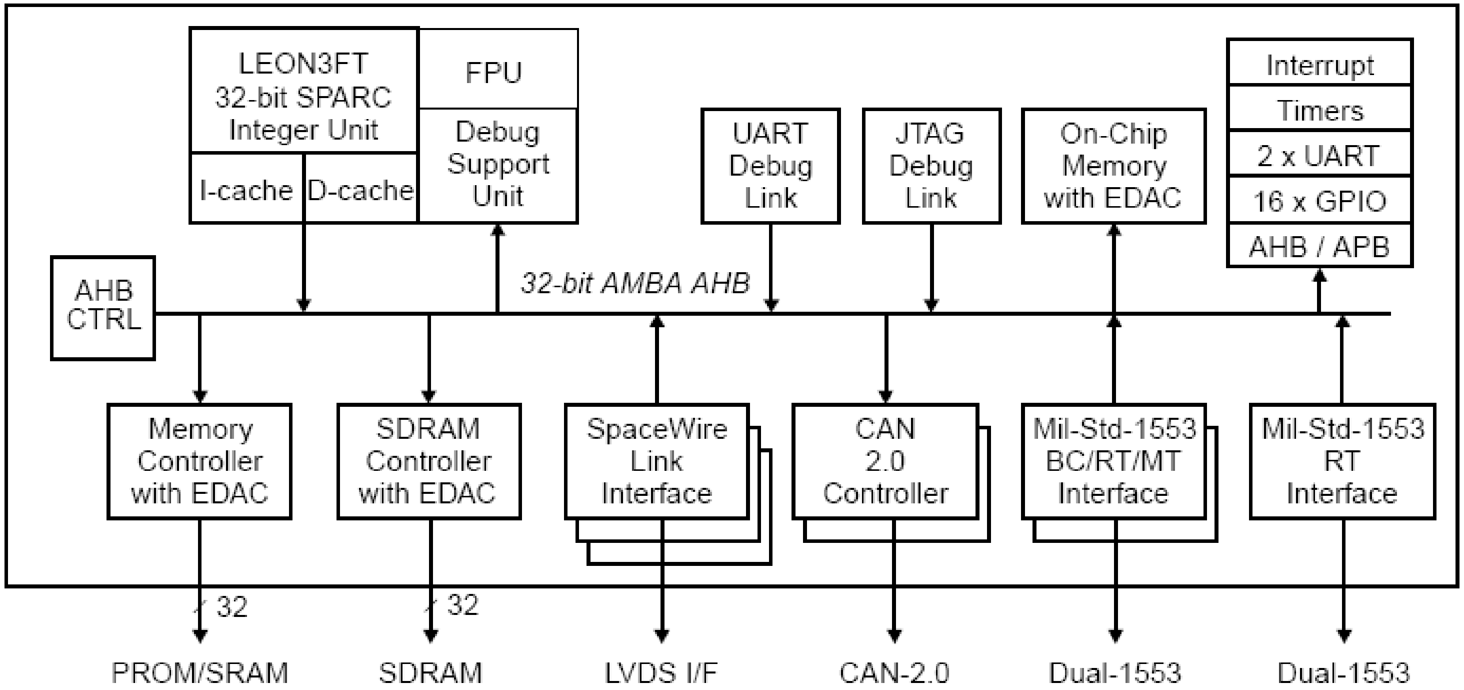
Present and next future :

- **AT697E-F**/Leon2 (SPARC V8 architecture 32 bits , Integrated 32/64-bit IEEE 754 Floating-point Unit, EDAC on chip, up to 86 MIPS, up to 100 MHz, up to 23MFlops 0.25um silicon lithography process by Atmel, 3.3 Vdc)

Present and future scenario

PROCESSORS USED in SPACE PROGRAMS (ESA, ASI) as CENTRAL CORE FOR PAYLOAD COMPUTERS (cont'd):

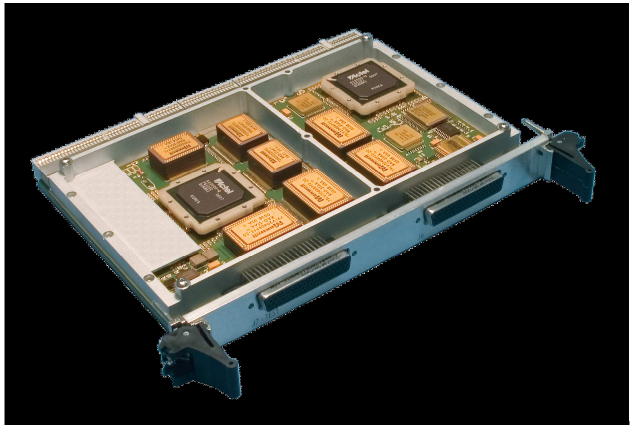
- **Leon3** (SPARC V8 architecture 32 bits , Integrated 32/64-bit IEEE 754 Floating-point Unit, EDAC on chip plus multiple SpaceWire links, CAN 2.0 and MIL-STD-1553B) VHDL core available to be synthetized into a FPGA/ASIC (System on Chip) see www.gaisler.com

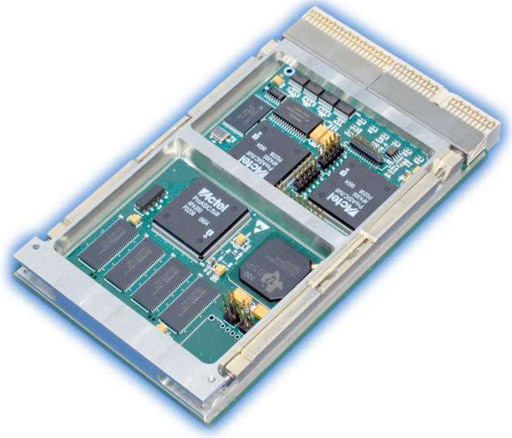


Present and future scenario

PROCESSORS USED in SPACE PROGRAMS (ESA, ASI) as CENTRAL CORE FOR PAYLOAD COMPUTERS (cont'd):

- **COTS** (Commercial off the shelf) solution as SCS750 6U cPCI board from Maxwell Technologies (www.maxwell.com) based on three PowerPC750FX running @ 800MHz, S210 or S950 from Aitech (www.rugged.com) that are a VME and a cPCI board based on PowerPC750 or the Proton200kFt/Fx cPCI Board from SpaceMicro Inc.(www.spacemicro.com) based on Texas Instruments 'C6xxx DSP family (320C6415 1GHz-4000MIPS,320C6713 300MHz-900MFlops)





SCS750 from Maxwell S950 from Aitech Proton 200k from SMI

Present and future scenario

PROCESSORS USED in SPACE PROGRAMS (ESA, ASI) as CENTRAL CORE FOR PAYLOAD COMPUTERS (cont'd):

Future:

As outlined at the Next Generation DSP round table during the ADCSS07 conference (November 07, ESA-ESTEC) several solutions are currently under evaluation: from the hardening of COTS processor against radiation effect using a RAD HARD tech at die level (i.e. 'C67xx from TI as made for the TSC21020 from Atmel that is based on the '21020 of Analog Devices) to a multicore solution based on a combination of Leon3 core with DSP IP core.

Present and future scenario

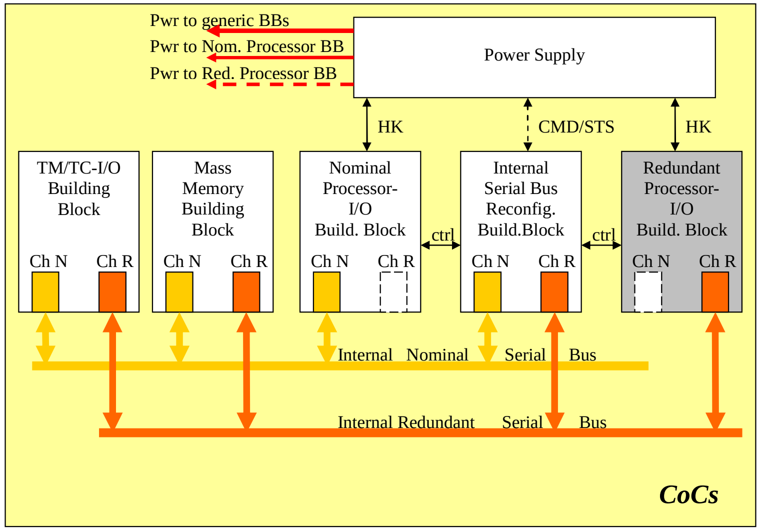
PROCESSORS USED in SPACE PROGRAMS (ESA, ASI) as CENTRAL CORE FOR PAYLOAD COMPUTERS (cont'd):

Future:

ESA-ESTEC (Tech Division) has recently released a ITT (AO5654) for the development of a "High Performance COTS based Computer for Payload systems" (HI-P CoCs) based on Cots components/parts and to be used for future Scientific Mission.

Its features should be:

- Lifetime: 15 years,
- Performance: > 500 MIPS or >500MFLOPs,
- Based on building blocks,
- HI-P CoCs I/Fs: 3 high speed bus (> 300 Mbits, to be used as communication links with the instruments on one side and with the Mass Memory Unit on the other) - 3 low speed bus (of the class 1 Mbit per second, to be used as Control & HK I/F)



Present and future scenario

TI's DSP 'C67xx Architecture

VLIW (256 bits) to supply up to 8 32-bit instructions to 8 Functional Units

Two sets of Functional Units: L, S, M and D

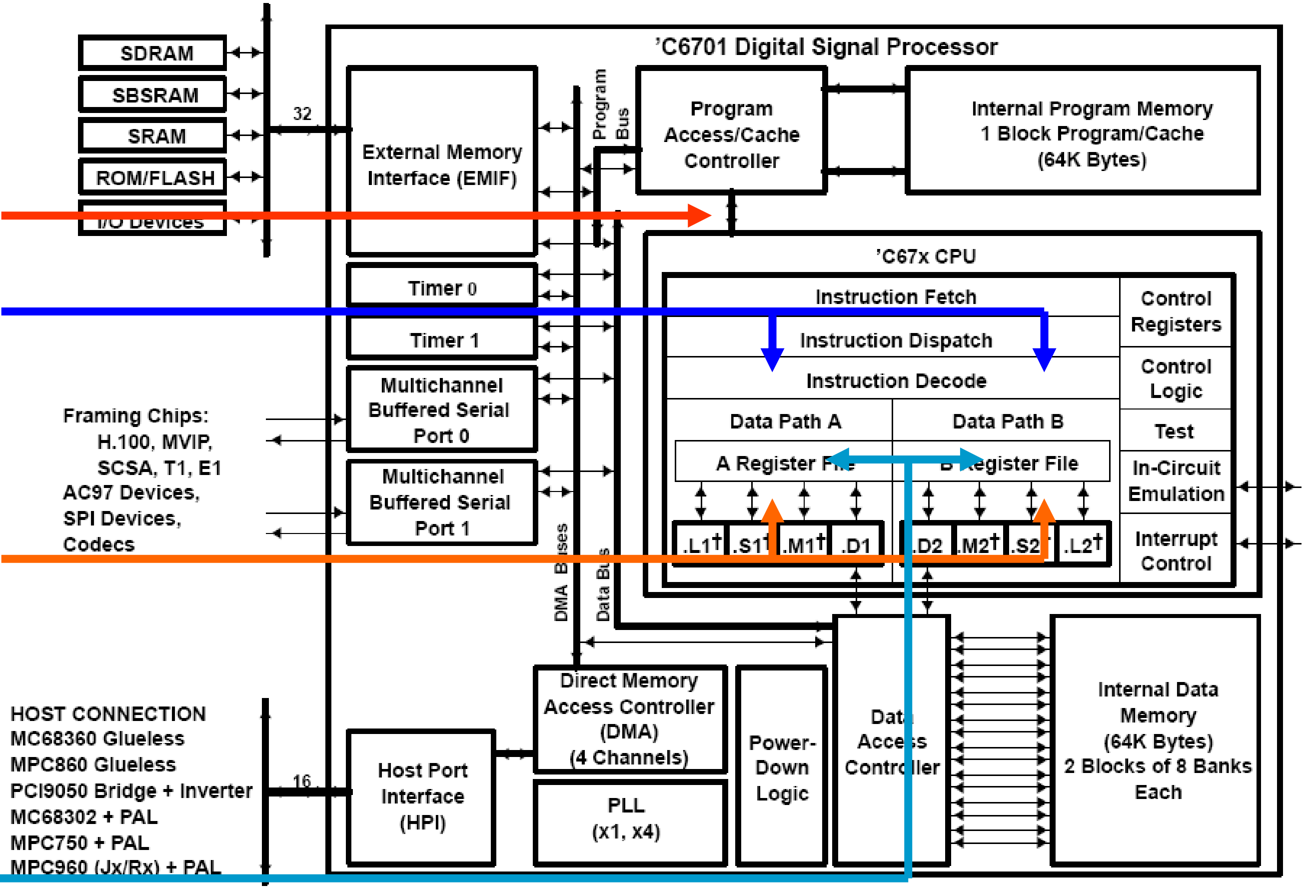
Two register files (A and B), each contains 16 (32 for 'C64xx) 32-bit registers for a total of 32 (64 for 'C64xx)

L,S= performs arithmetic, logical, and branch functions

M= performs Multiply Op.

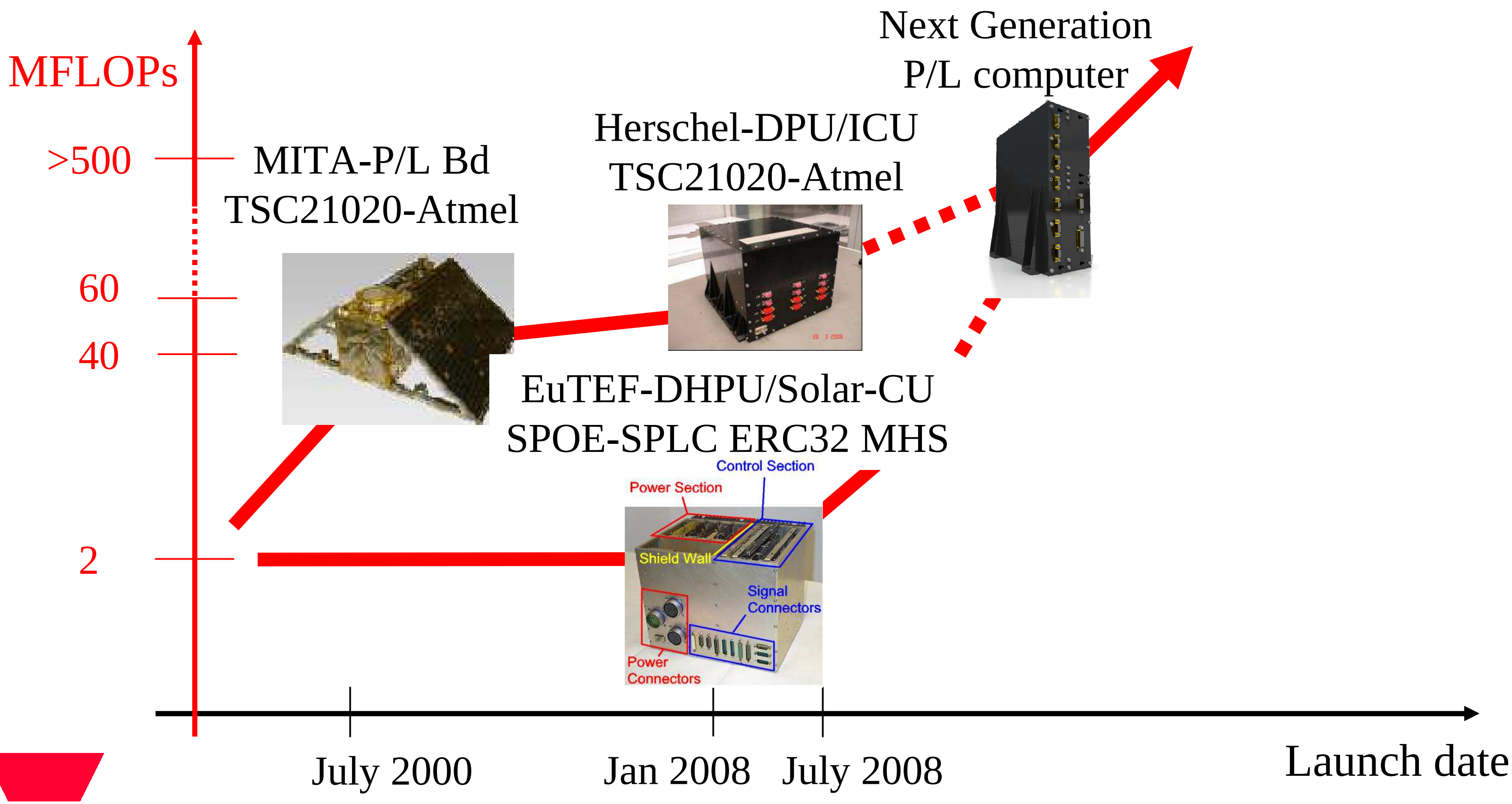
D = performs Data Transfers

Data Cross Path Between the Two Register Files

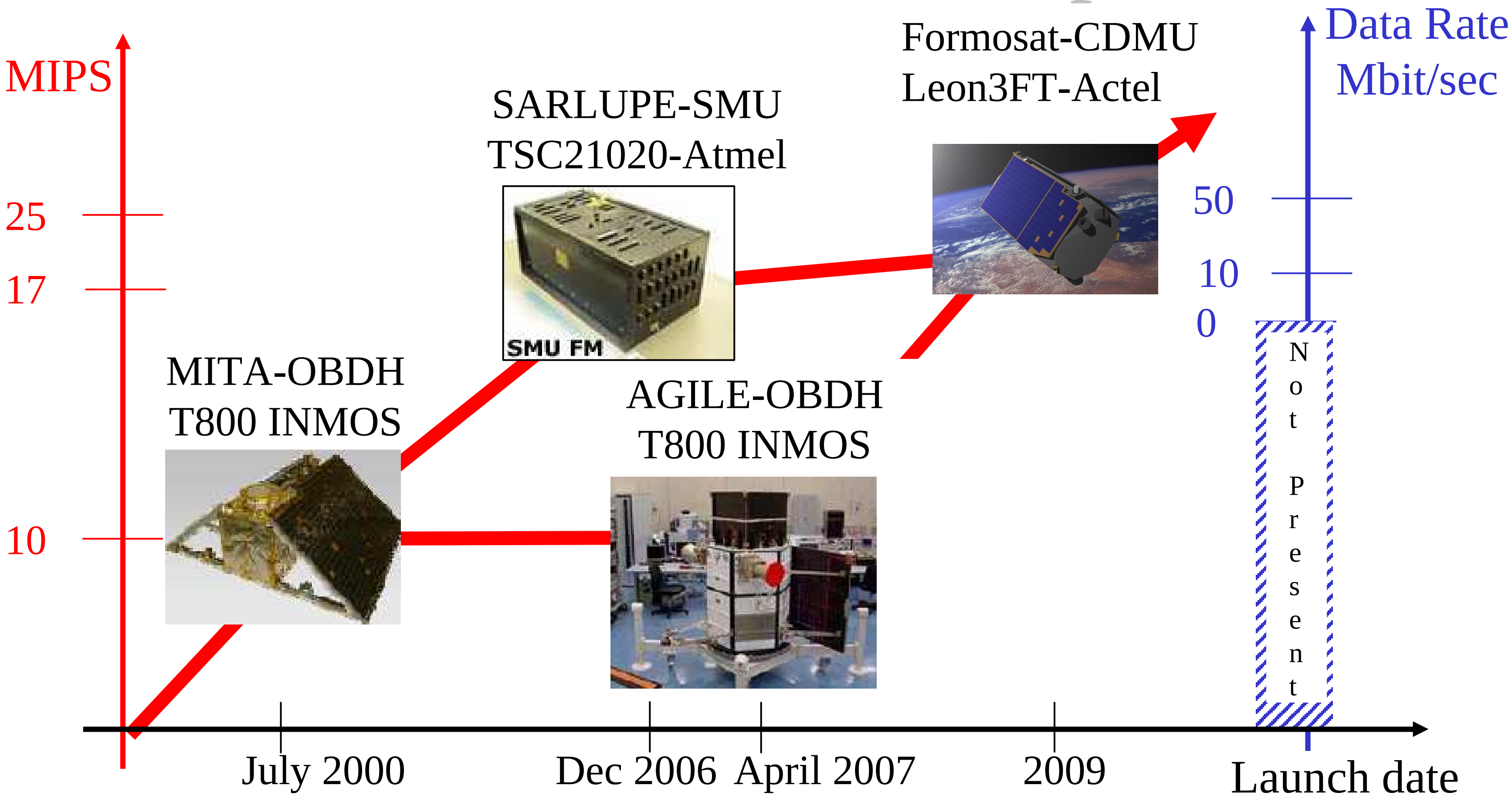


† These functional units execute floating-point instructions.

CGS P/L Computer Roadmap

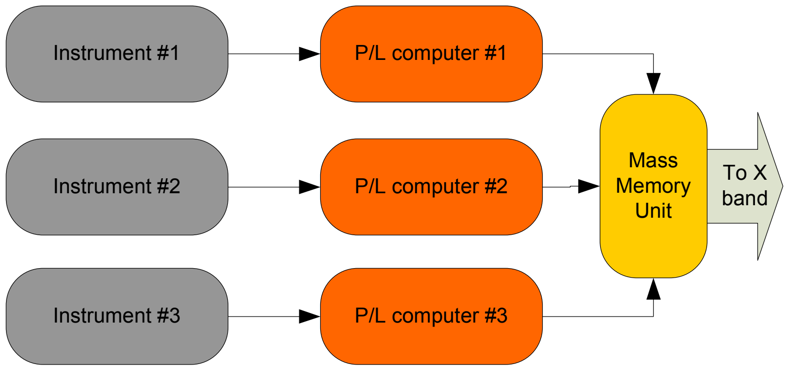


CGS OBDH Roadmap



Fast digital Interfaces

Fast digital interfaces are needed to implement the data flow among the detectors and the P/L computer(s), between the P/L computer(s) and the Mass Memory Unit and finally between the Mass Memory Unit and RF (X) Transmitter.



Currently data throughput up to several hundreds (and in some cases also some thousands) of Mbit/sec are commonly required.

Serial transmission on copper path with specific protocols (HW and SW) developed in order to endure the error detection and correction functionality (parity bits, packet checksum, hot redundancy, re-transmit on error, …) is commonly used.

Special care is spent in order to increase the noise immunity and to minimize the EMI interferences (galvanic isolation, twisted and double shielded cables, differential signalling,….).

Fast digital Interfaces

Which are the most common used fast serial I/Fs in the scientific satellites or spacecrafts?

Commercial I/Fs have been and are used :

It's the case of the Ethernet on the International Space Station (Ethernet is galvanically isolated by means of transformers, 10Mbits/s now and 100Mbit/s in the future are the maximum speed), Taxi-HRDL (High Rate Data Link) running @ 125MHz with a capability to transfer unidirectional data at a maximum speed of 32.426 Mbit/sec, AC coupled) for Video signal again on the International Space Station.

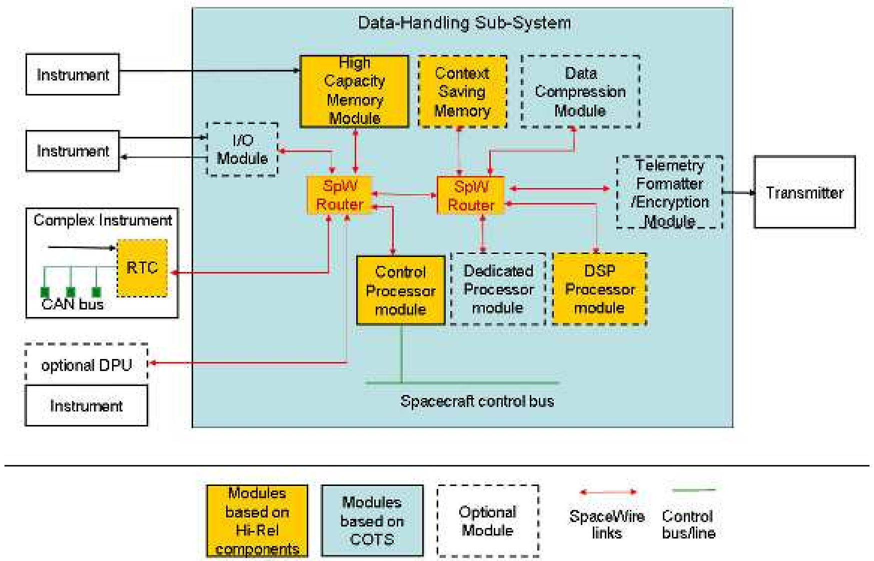
Gigalink from Agilent or HOTlink from Cypress Semiconductor are used as fast communication I/Fs on scientific satellites.WizardLink from TI is another interesting solution (available in ruggedized and radiation tolerant version).

Beside the various "commercial" choices a fully space qualified solution is available and is emerging: **SpaceWire**. It has already been used or selected to be used on many space missions (Herschel, GAIA, JWST, BEPI COLOMBO,…) and by many nations and international organizations (ESA, NASA, JAXA) and many European industries (and among them also CGS).

Fast digital Interfaces

Which are the benefits of the SpaceWire?

➢ Spacewire is a digital I/F developed to connect sensors , mass-memories , processing units, downlink telemetry sub-systems of a generic spacecraft and possibly in the future mission it could be the unique digital I/F present on a spacecraft (see the following architectural block diagram present on the SpaceWire page of the ESA website). Point to point connections but also arbitrary topology network based on SpaceWire routers are feasible,



ESA image

Fast digital Interfaces

➢ SpaceWire falls into an ESA standardization (**ECSS-E-50-12A)**,

➢ The SpaceWire Interface can be easily accommodated into an ASIC or FPGA (IP cores are available) and space qualified components produced by an European foundry are available (Atmel) , consequently an extended usage of this I/F also by small medium companies involved in the space market is easy to be conceivable,

➢The use of the SpaceWire standard can ensure that equipment is compatible at both the component and sub-system levels. Processing units, mass-memory units and down-link telemetry systems using SpaceWire interfaces developed for one mission can be readily used for other missions or just with little modification (architectures based on building blocks). This means a reduction of the cost of project development, a reduction of the development schedule and an improvement of the design reliability and project confidence,

Fast digital Interfaces

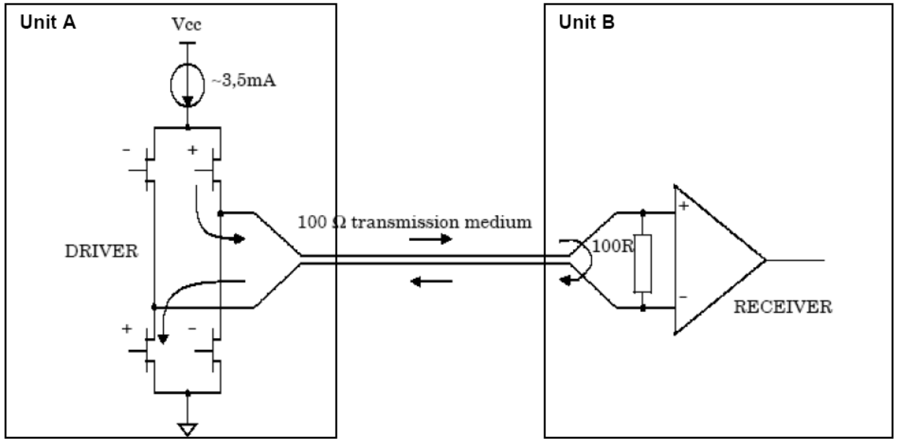
➢ ESA is also accompanying the deployment of SpaceWire networks by defining, in coordination with other organization like NASA, JAXA and Roscosmos, higher level protocols aimed at further extending the capability of SpaceWire to build modular and easy to assemble on-board data systems.

➢ Furthermore ESA is also working on evolution of the SpaceWire (SpaceFibre) to extend the data throughput in order to be compliant with possible future higher demanding needs: definitively SpaceWire is a technology that is currently available but it is also looking in the future.

Which are the characteristics of the SpaceWire?

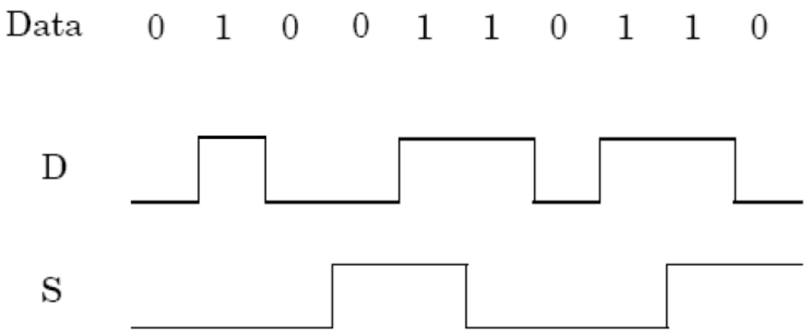
Serial, low voltage differential signalling, high-speed (from 2 Mbits/sec to 200 Mbits/sec), bi-directional, full-duplex I/F.

See the adjacent scheme (Additional power up and down resistors can be placed at the receiver end.



Fast digital Interfaces

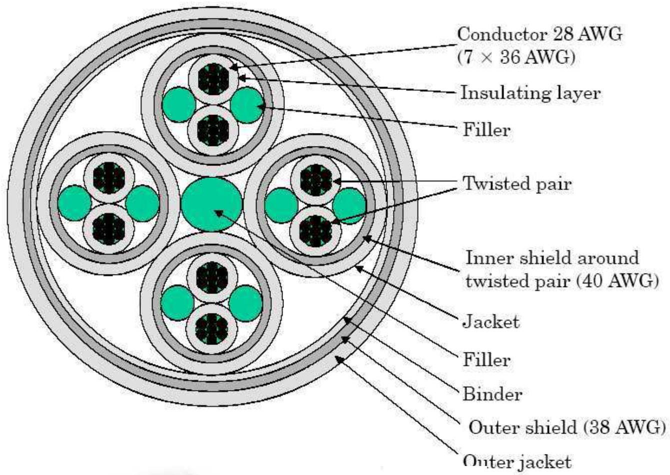
The signal levels and noise margins for SpaceWire are defined taking into consideration the ANSI/TIA/EIA-644 specifications that defines the driver output characteristics and the receiver input characteristics of LVDS devices.
SpaceWire uses Data-Strobe (DS) encoding. This is a coding scheme which encodes the transmission clock with the data into Data and Strobe so that the clock can be recovered by simply XORing the Data and Strobe lines together. The data values are transmitted directly and the strobe signal changes state whenever the data remains constant from one data bit interval to the next. This coding scheme is illustrated in the following diagram.
The DS encoding scheme is also used in the IEEE Standard 1355 and IEEE 1394 (Firewire) Standard.



Fast digital Interfaces

A SpaceWire link comprises two pairs of differential signals, one pair transmitting the D and S signals in one direction and the other pair transmitting D and S in the opposite direction. That is a total of eight wires for each bidirectional link.

The SpaceWire cable has to be constructed according to ESA ESCC 3902/003 specification and comprise four twisted pair wires AWG28 with a separate shield around each twisted pair and an overall shield as illustrated in the adjacent figure



The SpaceWire connector is a nine contact micro-miniature D-type as defined in ESA ESCC 3401/071 specification

Fast digital Interfaces

No drawbacks in using the Spacewire?

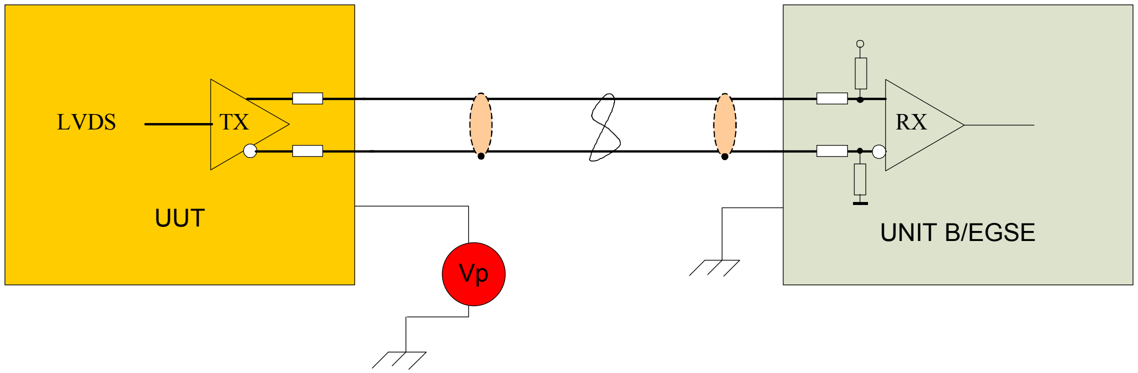
Currently no galvanic isolation (through means of signal transformer as in MIL-STD- 1553B or Ethernet) is foreseen by the SpaceWire physical layer and consequently a theoretical lower immunity to EMC interferences w.r.t for example a MIL-STD-1553B I/F is conceivable.

Here we want to mention the EMC/ESD Control Plan & Procedure of the PACS instrument (that is one of the three Instruments of the ESA Herschel mission) where the 1355 interface that is the industrial version of the SpaceWire and from which the SpaceWire has been derived maintaining the electrical characteristics, has been used.

In this document there is a description and as sort of guiding rules for all the EMC test sessions to be performed and, among them, our attention has been captured by the Common Mode Conducted Susceptibility Test procedure on signal reference.

Fast digital Interfaces

The test has to be performed on each unit disconnecting the bonding strap of the UUT and applying a signal transient between the UUT signal reference (bonding stud) and the ground plane and verifying that the UUT does not exhibit any malfunction, degradation or performance.
A note specifies that in the case the UUT uses a digital interface with LVDS drivers and receivers (as the 1355/SpaceWire does) the peak amplitude of the transient to be applied has to be reduced down to 1.2V in order to take into account the reduced CMRR of the LVDS Receivers and Drivers. Basically this means a lower noise and disturbance immunity of the 1355/SpaceWire I/F wrt other digital Interfaces.

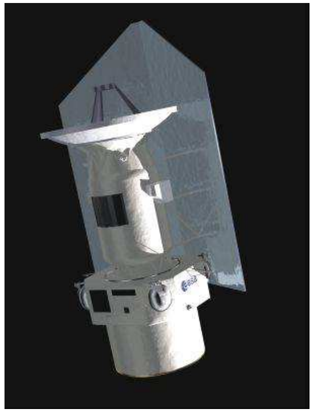


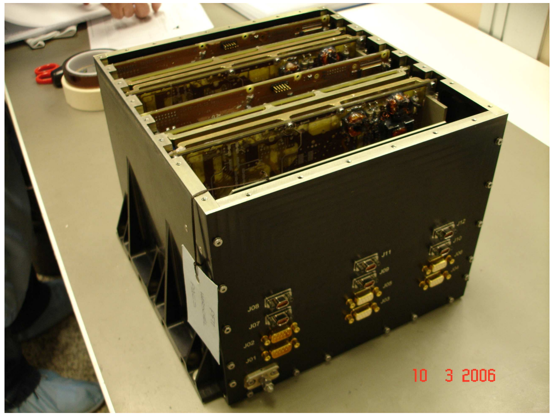
EMC test on Flight Units

Which are the typical EMC tests that are performed on a flight unit in stand-alone configuration ?

Here after we list the EMC tests of the Herschel DPU/ICUs (Data Processing Units/Instrument Control Unit of the three Instruments of the Herschel Satellite):

- Bonding,
- Conducted Emission on Unit Primary lines, Differential and Common Mode, (Frequency range 10kHz-50MHz),
- Current Ripple on Unit Primary lines (time domain),
- Inrush on Unit Primary lines,





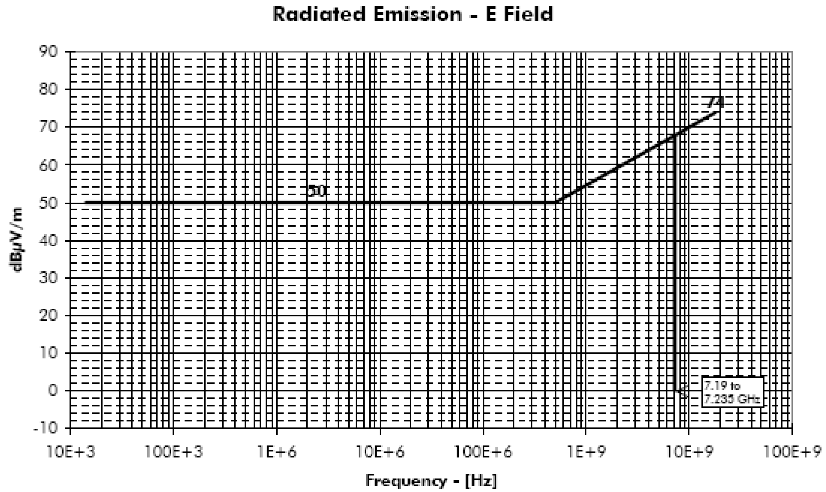
EMC test on Flight Units (cont'd)

Which are the typical EMC test that are performed on a flight unit in stand-alone configuration ?

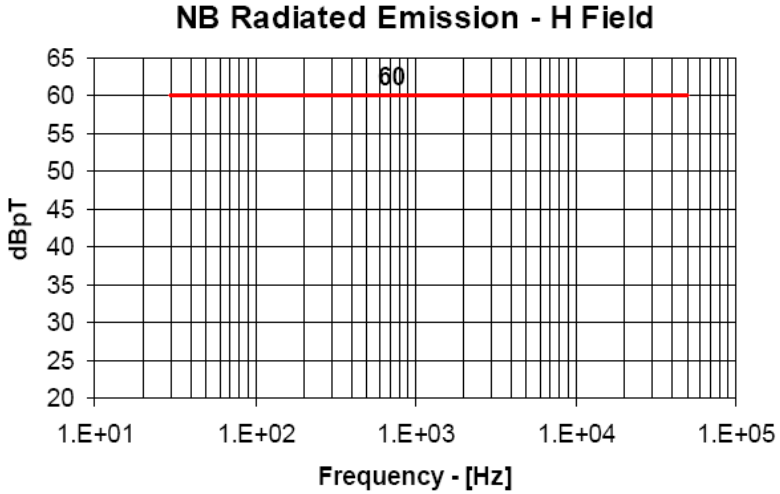
- In case of provision of power outlets (Herschel HIFI ICU) : ripple, spike and common mode current (e.g. limits are 10µArms, at 10KHz; Increasing 20dB/decade until 1mArms at 1MHz; 1mArms between 1MHz and 10MHz in case of the Herschel HIFI Instrument Control Unit),
- Conducted Susceptibility on Unit Primary lines, Differential and Common Mode, Frequency and Time domain (Frequency range 10kHz-50MHz),
- Conducted Susceptibility Common Mode Voltage on Signal Reference frequency and time domain,
- Signal isolation on Digital I/F,

EMC test on Flight Units (cont'd)

Which are the typical EMC test that are performed on a flight unit in stand-alone configuration ?



➢NB E-FIELD RADIATED EMISSION 14kHz – 18GHz



➢NB H-FIELD RADIATED EMISSION 30Hz – 50kHz

EMC test on Flight Units (cont'd)

Which are the typical EMC test that are performed on a flight unit in stand-alone configuration ?

- NB E-FIELD RADIATED SUSCEPTIBILITY: UUT shall be irradiated with 2 V/m, 1 kHz amplitude modulated (30% AM), in the frequency range 14 kHz – 18 kHz, and 10 V/m from 8.45 GHz to 8.5 GHz (spacecraft TM)
- NB H-FIELD RADIATED SUSCEPTIBILITY: UUT shall be irradiated with a magnetic field of 140dBpT in the frequency range 30Hz – 50kHz

What is missing in the required EMC tests session performed at unit Level or left at EMC test to be performed at integrated/system level?

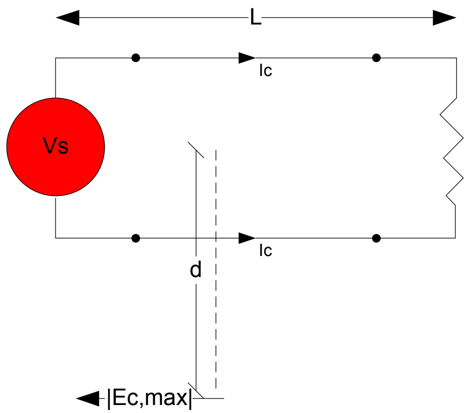
- Direct measurements of common mode current flowing on cables that carry digital signals,
- EMC Intra-Compatibility among the various units that compose the system-satellite

EMC test on Flight Units (cont'd)

Which is the relationship between a common mode current flowing on a cable and the generated Electric Field?

$$|E_{c,max}/I_c| = K*L*f$$ [1)]

Where Ec is the Electric Field, Ic is the current flowing in the cable , K = 1.257E-6/d where d is the distance at which the measurement is taken (3 mt for FCC, 1mt for Space tests session) , L is the cable length and f is the frequency.



Considering a cable with a length of 1mt, a common mode current of 8uA is able to provide a Electric Field of 50dBuV @ 30MHz that is equal to the limit.

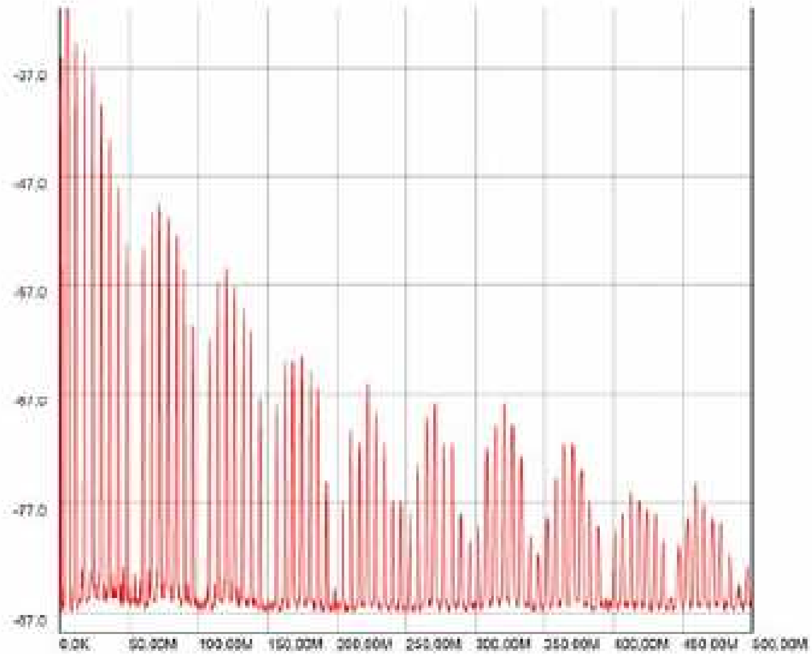
1) See chapter 8 of "Introduction to Electromagnetic Compatibility", Clayton R. Paul John Wiley and Sons, Inc or the italian translation "Compatibilità Elettromagnetica" by Hoepli.

EM Emission: a minimization technique

Dr Barry M. Cook and Paul H. Walker of the 4Links Limited company (www.4links.co.uk) have presented an interesting paper at DASIA2007 (*DAta Systems In Aerospace Conference), Naples, Italy, 29 May - 1 June 2007)* titled "REDUCING ELECTROMAGNETIC EMISSIONS FROM SPACEWIRE".

They have measured the emission spectrum generated by a system consisting of a SpaceWire module feeding 2.5m cable with a loopback connector at the end (total SpaceWire round trip of 5m).

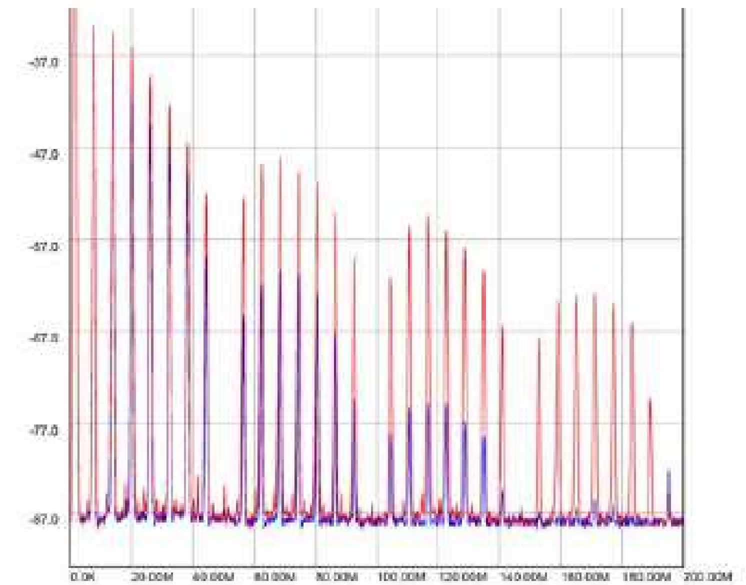
The speed of the Spacewire links was 49 Mbit/s. The lowest frequency is at 6MHz (49MHz / 8-bits being 8 bits the extension of the NULL packet) with signals at multiples of that frequency



EM Emission: a minimization technique

The proposed first type of emission reduction is through the “Edge Control”.

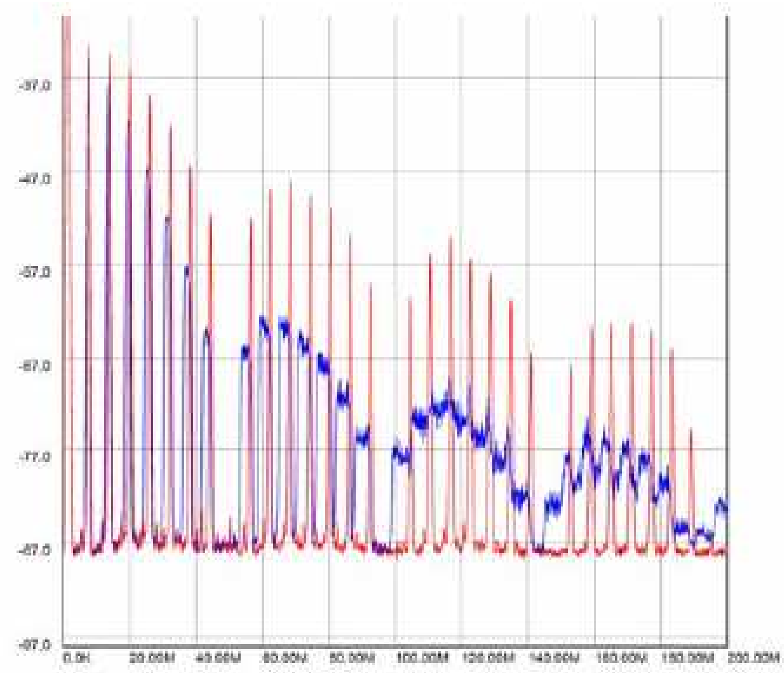
For a data rate of 49Mb/s the bit-period is 20ns and although rise/fall times should be a fraction of this, typical LVDS buffers are an order of magnitude faster than is necessary (300psec as rising/falling time) . Such over-capability provides an increased working margin for the designer but at the expense of a greatly extended emission spectrum. The suggestion from 4Links Lim. is to tune the driver characteristics to the project speed clock controlling the rise/fall time by a capacitive loading: in the adjacent figure the behavior with (blue) and w/o (red) a 100pf capacitance across each transmit pair is shown.



EM Emission: a minimization technique

Another type of conceivable emission reduction proposed by 4Links Lim. is through the “Rate Randomisation ”.

SpaceWire, with its direct clock recovery of the receiver through XOR-ing of the D and S signal , has no need to use phase-locked-loops and puts no restriction on the rate of change of input data rate. It is perfectly allowable from a theoretical point of view for the data rate to change from one extreme (2Mbit/s is the minimum) to the other (200Mbit/s) this technique commonly used is known as spread-spectrum-clocking. This spreads the energy of single-frequency spikes over a range of nearby frequencies and reduces the peak levels significantly. See the result in blue in the adjacent figure.

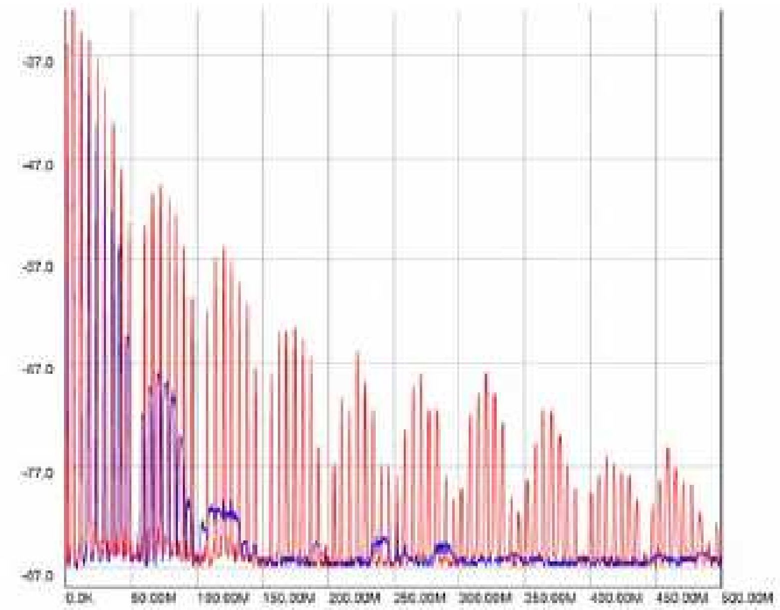


Reductions of 3 to 12dB are obtainable just considering a spread of 4% of the data rate

EM Emission: a minimization technique

Combined approach: “Edge control” and “Rate Randomisation ”.

Using both edge control and spread-spectrum clocking or rate randomisation (or spread-spectrum-clocking) techniques the result is a very significant reduction in the generated spectrum and thus reduced emissions within the satellite. Reduction figures up to 20db are achievable (with a 4% spread spectrum clocking and 100pF rate control capacitive loading at the LVDS transmitter output applied).



ARES-EMC: an analysis tool

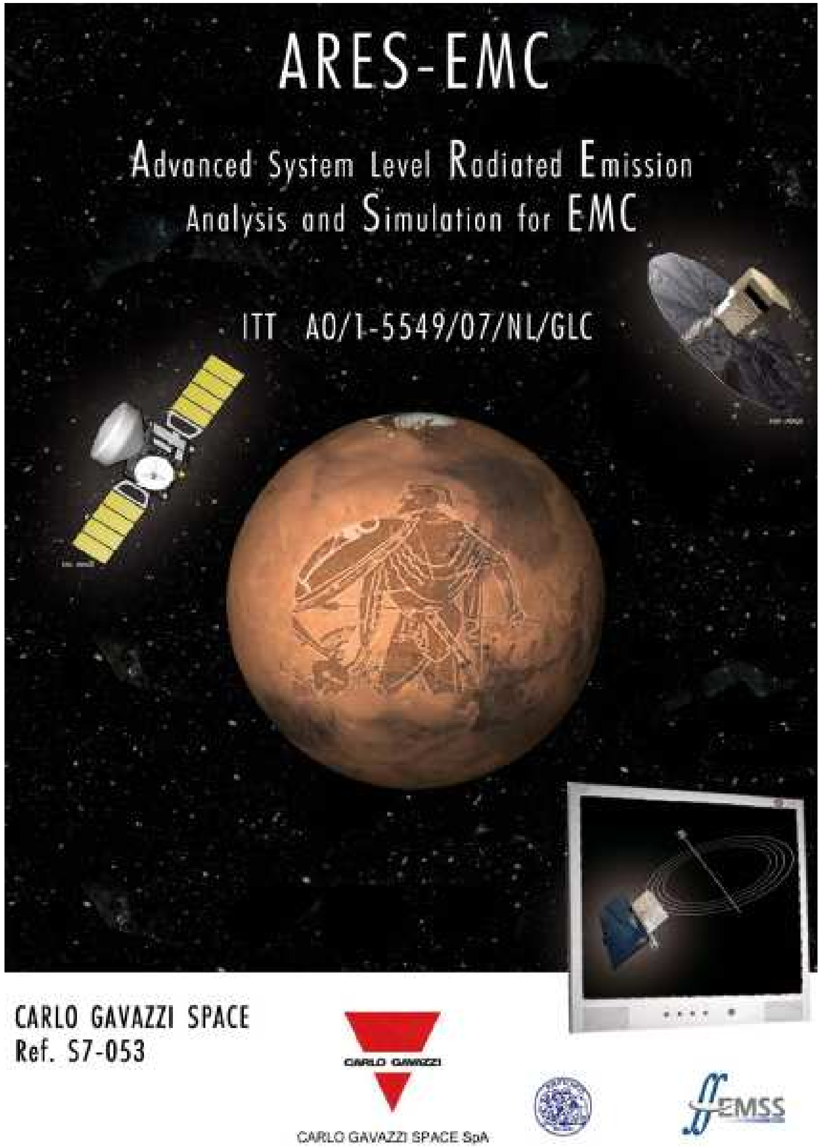
Carlo Gavazzi Space has positively closed the negotiation phase with ESA for the ITT AO/1-5549 "**A**dvanced System Level **R**adiated **E**mission Analysis and **S**imulation for **EMC**" that has as final scope the development of a tool for "system level susceptibility analyses" capable to treat field-to-wire coupling problems in a satellite.

The ITT has been issued by the directorate of TEC (EMC session)

The project team sees also as subCo:

EMSS GmbH. Software solutions for the simulation of electromagnetic fields.

Politecnico di Milano (Dipartimento of Elettrotecnica)



ARES-EMC: objective

The Objective of the Invitation to Tender “Advanced System Level Radiated Emission Analysis and Simulation for EMC” is of relevant interest for several reasons:

- To allow an early verification of intra-spacecraft EM compatibility among power, data and P/L units when no real units are still available,
- To drive the design of the units and the harness routing in the spacecraft considering also EMC issues,
- The availability of a SW tool that allows the space agencies and the satellite/prime contractors to evaluate possible Non conformances or Requests for Waiver risen by subcontractors simulating their impacts on the (not existing yet) satellite,
- The risk reduction related to the EMC System level tests that are usually performed at the final phase of a space program

ARES-EMC: objective

The current situation concerning the availability of matured and validated software tools for the analysis and prediction of the radiated susceptibility in complex systems like a spacecraft in the low-medium frequency range is quite unhappy but….

The maturity reached by software tools in the high frequency range of the EM fields that allows their use in telecom satellite acts as a strong stimulus to try to develop and validate a software system tool that can provide helpful information to the space architects/designers/specialists in all the phases of the development activity of a satellite considering the randomness and the uncertanties of the system to be analyzed in term of EM sources, victims and structures.

ARES-EMC : Architecture

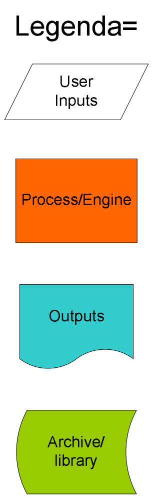
Architecture: our System Tool is composed of a custom development of an Analytical Tool based on the SPLS Software tool of Orcad/CADENCE and Mathworks tools (Matlab/simulink) integrated with the FEKO EM solver developed by EMSS.

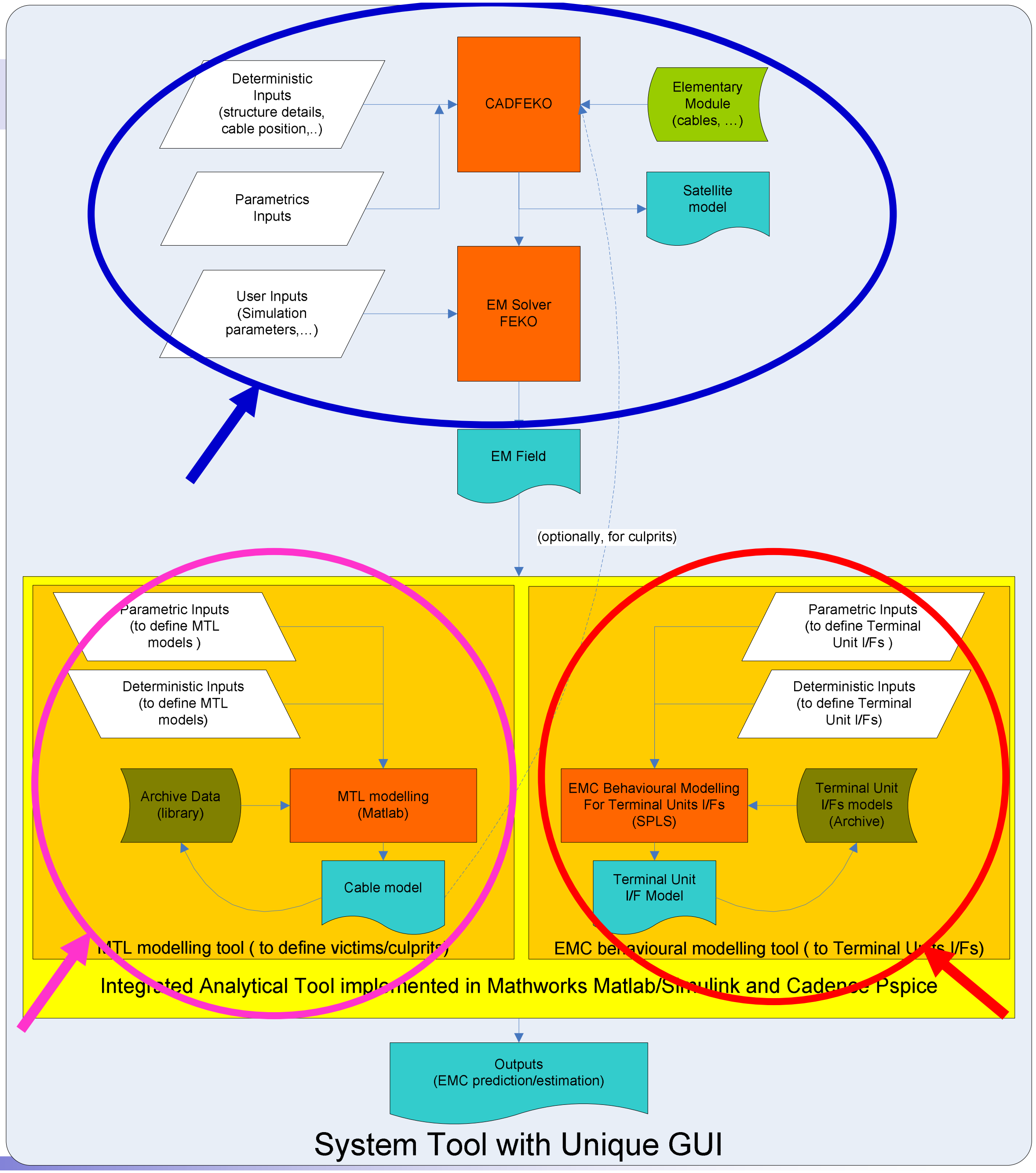
Components:

Modelling of Structure and EM Field,

Modelling of harness,

Modelling of Terminal I/Fs

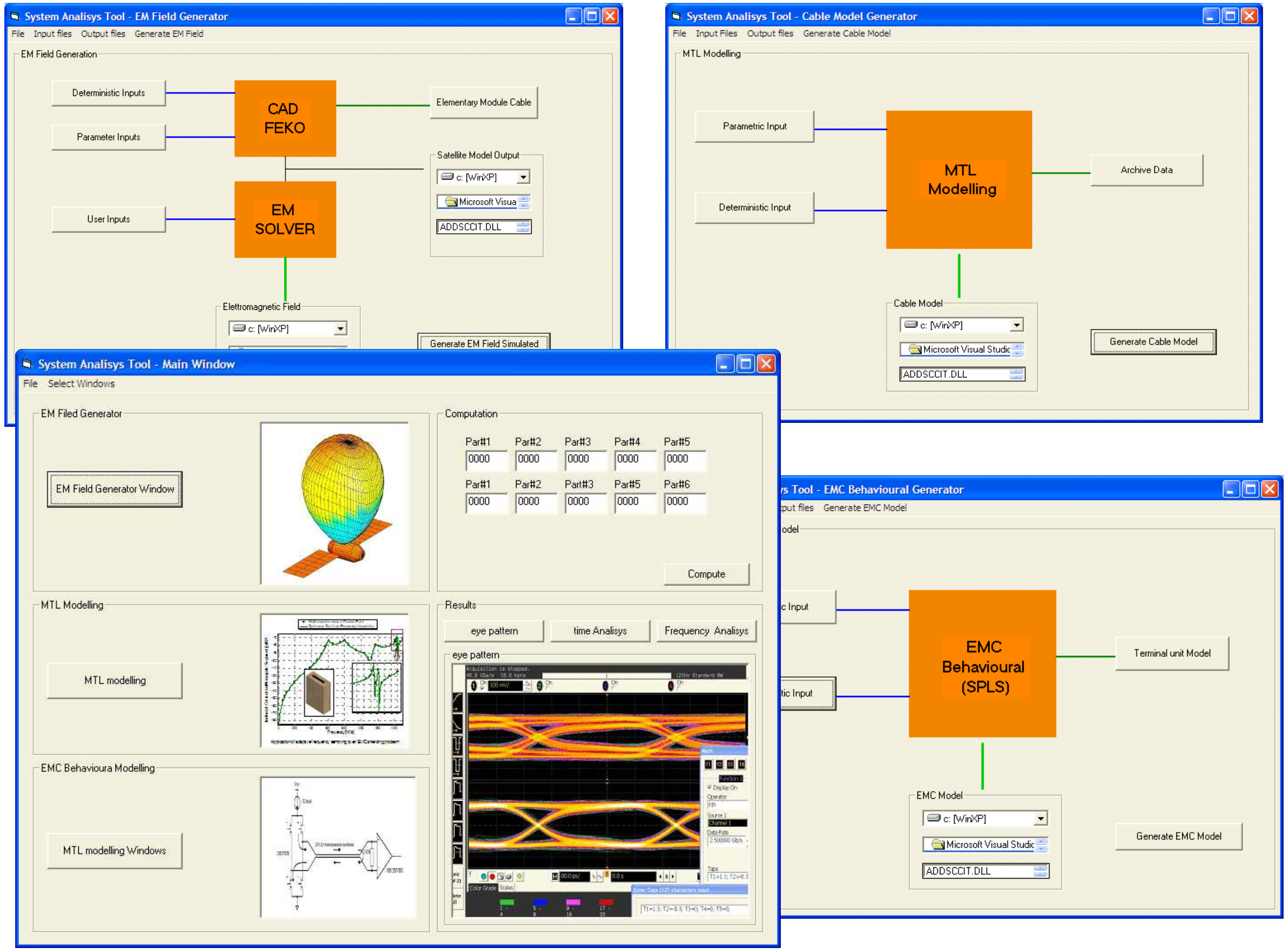




ARES-EMC: architecture

GUI

A friendly and unique graphical interface will guide the tool users through all the menus, parameters and types selections, already available library models, new models saving options of the provided System Tool.



System Tool GUI

ARES-EMC: architecture

In order to validate the System Tool some test cases will be studied, simulated and tested: within the digital buses commonly used in space the proposal team has identified the following as the ones to be investigated:

RS422

SpaceWire

The RS422 represents a low-medium speed solution that has found a diffusion as low-cost, easy to use and robust enough I/F to control and monitor P/Ls with a limited data bandwidth request,

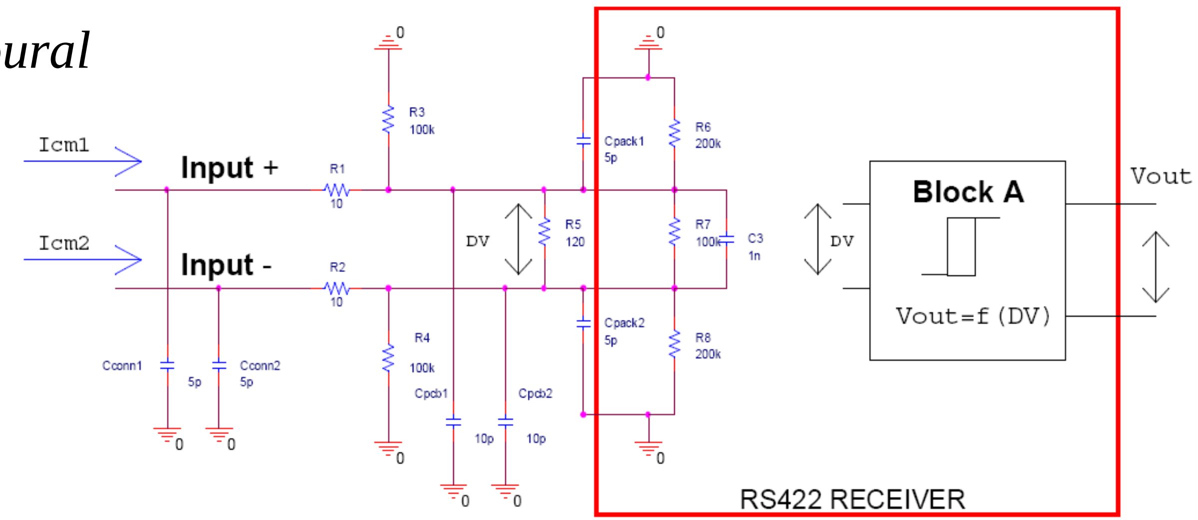
The **SpaceWire** is the leading data-handling network for use onboard spacecraft, furthermore the SpaceWire falls into an ESA standardization and finally the use of the SpaceWire standard can ensure that an equipment is compatible at both the component and sub-system levels. Processing units, mass-memory units and down-link telemetry systems using SpaceWire interfaces developed for one mission can be readily used for other missions.

ARES-EMC: architecture

The EMC behavioural model of the SpaceWire I/F will be developed: the behavioural model will be implemented using the CADENCE PSpice Simulator and Mathworks' Matlab/Simulink.

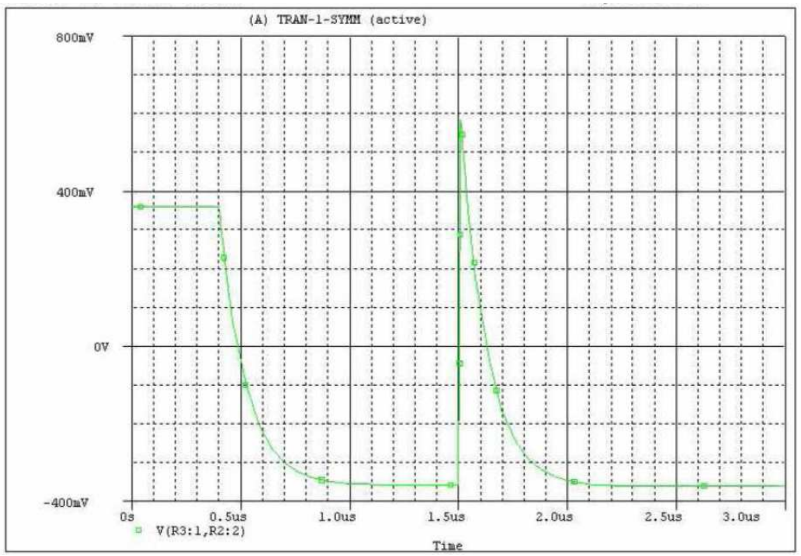
The modelling of EMC parasitic effects will be obtained starting from suitable experimental characterization that will be combined with the functional model of the Terminal Units Interfaces.

Example of EMC behavioural model (RS422)



ARES-EMC: architecture

Simulation and validation test shall be performed in order to verify for example the effect of common mode noise in case of balanced or unbalanced configuration.



Input of the Differential Receiver in case of common mode noise/spike in presence of a balanced (left) or unbalanced configuration (right)

ARES-EMC: architecture

The behavioural models will include the following features:

- Possible non linear behaviour of the termination in the full range of operability (from 2 to 200 Mbit/s as data rate for SpaceWire) that can be treated by means of multiple linear models to be associated with different frequency ranges.
- Statistical treatment of the system uncertainties (parasitic impedance to chassis ground, parasitic capacitance between path "+" and "-" due to PCB and connector,…)
- To be suitable to be integrated in the selected EM field solver.

Furthermore it has to be underlined that the internal schematic or simulation model of a RS 422/SpW receivers is usually not available to the customers so CGS proposes to create a Parametric Macromodel of the RS 422/Spacewire receiver's core (see also IEEE TRANSACTIONS ON ADVANCED PACKAGING, VOL. 25, NO. 2, MAY 2002 Parametric Macromodels of Digital I/O Ports Igor S. Stievano, *Member, IEEE*, Ivan A. Maio, *Member, IEEE*, and Flavio G. Canavero, *Senior Member, IEEE*)

ARES-EMC: architecture

Substantially the Parametric Macromodel methodology aims to obtain a representations of the IC behaviour starting from the measurement of transient waveforms at the device ports.

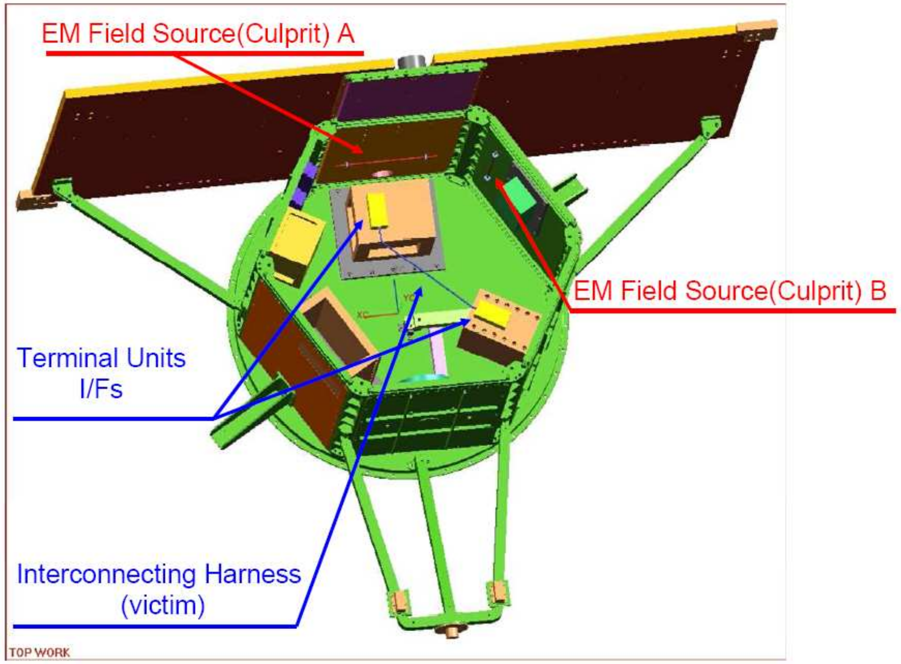
The parametric approach to behavioural modelling has interesting features if compared to the traditional equivalent circuit simulation. It can take into account any physical effects significantly influencing voltages and currents of the IC ports and yields models that perform at a very good accuracy level with relatively high efficiency (in term of required computational time).

Furthermore depending on the frequency components present in the stimulus the transfer function of the RS 422/SpaceWire receiver can be investigated in all the frequency bandwidth of interest also well behind the nominal bandwidth of the receiver and taking into account the eventual nonlinearities of the device core.

Currently analyses using the System Identification Tool of Matlab and the Parameter Estimation Tool of Simulink are on going.

ARES-EMC: validation

One of the most important phases of the work to be developed is the validation of the system tool: It will performed on a metallic mock-up of the italian AGILE satellite and real EM Field sources and Terminal Unit I/Fs will be used.



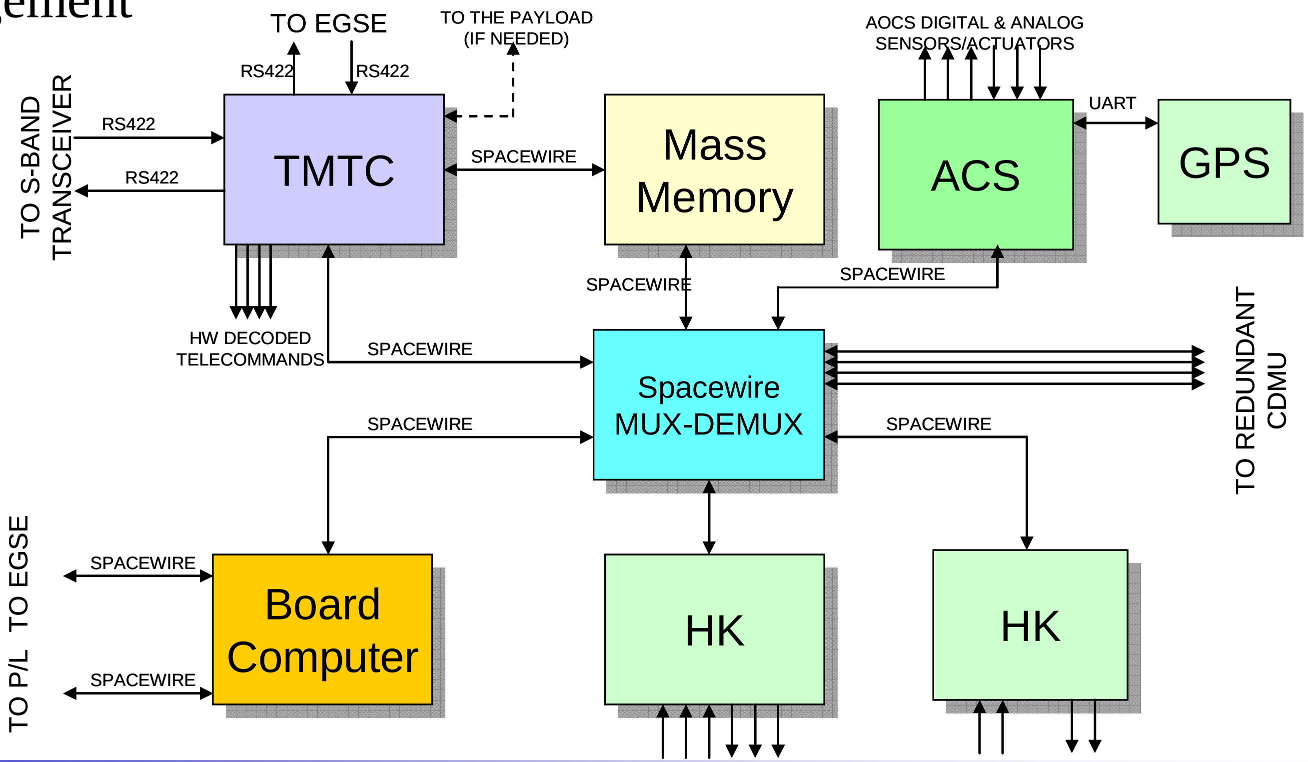
A possible application in CGS of ARES-EMC: CDMU

Carlo Gavazzi Space is currently involved in the final testing phase of the Formosat-X (former ARGO) CDMU for the the National Space Organization (NSPO) of Taiwan.

The CDMU (**Command and Data Management Unit)** main tasks are:

- On Board Data Handling
- Attitude and Orbit Control
- Payload Management

CDMU ARCHITECTURE



Conclusions

- The present and the next generation of P/L computers and scientific satellites see a dramatic increase of the design complexity and speed of the digital units,
- Fast digital I/Fs (COTS but also space qualified as SpaceWire) are used to transfer huge amount of data,
- The SpaceWire bus is one of the most diffused digital I/Fs on the scientific satellites.
- Wih the increase of the speed and the number of the flight digital interfaces, issues related to the EM emission and susceptibility have to be taken into account, some design solutions and or analysis tool are and will be available trying to reduce the potential problems.

THANK YOU !