Mulitphysics Solution for Nanoelectronics

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Real World: Multiphysics

Create So Many Chances for All of Us

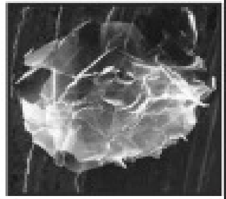
Call for Papers

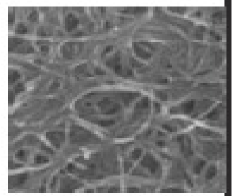
IEEE Transactions on Electromagnetic Compatibility
Special Issue on
Applications of Nanotechnology in Electromagnetic Compatibility (Nano-EMC)
Papers must be submitted by May 1, 2011

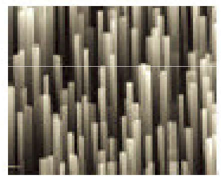
First Special Issue will be published in IEEE Trans. EMC

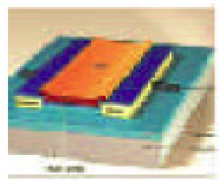
CALL FOR PAPERS
IEEE Transactions on Electromagnetic Compatibility

Special Issue on
Applications of Nanotechnology in Electromagnetic Compatibility (nano-EMC)









In the past few years, there has been an exploding interest in nanoscale science and technology. Nanotechnology is functional engineering on an extremely small scale that can be used to develop innovative materials and devices, and implants for numerous industrial applications. It involves the control of materials with a nanoscale fine structure, and with the manipulation of tiny objects at the dimension of molecules and atoms. The potential benefits of nanotechnology are revolutionary. Nanotechnology is truly multidisciplinary: research at the nanoscale frontier is unified by the need to share knowledge, tools and techniques, and expertise on atomic and molecular interactions. Nanotechnology is currently exploited in electronics, optoelectronics, photonics, sensors, material science, medicine and biology, but its application in EMC is still not very wide.

This Special Issue is intended to present recent research advances in nanoscale science and nanotechnology with applications of interest for the EMC community. The Special Issue is aimed to bridge the gap between nanoscale science and technology and EMC; to present new materials, devices and processes for EMC applications exploiting the powerful of nanotechnology; to investigate EMC issues related to the integration of nanocomponents in micro and macro electrical and electronic systems.

Suggested topics to be covered in this Issue include:

- Electromagnetic modeling and characterization of nanostructured materials, devices and systems for EMC;
- Nanostructured materials for EMC applications, like EM shielding, EM energy absorption, antistatics, surge suppression and protection, novel devices;
- Electrical and EM properties of nanocomposites for EMC;
- Nanointerconnects for next generation ICs;
- Signal integrity in nanocomponents and nanodevices;
- Nanostructured sensors for EMC;
- MEMS-based technology for smart antennas arrays and frequency-selective surfaces for EMC;
- Nanometrology for EMC.

IEEE Transactions on Microwave Theory and Techniques

Special Issue on

Radio-Frequency Nanoelectronics

Guest Editors

Luca Pierantoni, Università Politecnica delle Marche, Ancona, Italy
Fabio Coccetti, LAAS-CNRS Toulouse, France
Paolo Lugli, Technische Universität München, Germany
Stephen M. Goodnick, Arizona State University, AZ, USA

Call for Papers

Due to the new qualitative and quantitative improvements that nanotechnology allows, nanoelectronics has the potential to introduce a paradigm shift in electronic systems design similar to that of the transition from vacuum tubes to semiconductor technology. Since many nano-scale devices and materials exhibit their most interesting properties at radio-frequencies (RF), nanoelectronics represent an enormous and yet widely undiscovered opportunity for the microwave engineering community. However, these new concepts require theoretical and modeling foundations that are supported by established and sophisticated manufacturing and metrology capabilities. The issue at stake is paramount, to close the gap between the nano-science and a new generation of highly integrated and multifunctional devices, circuits, and systems in order to pave the way for a broad range of applications and operating frequencies, covering the RF spectrum, through the microwave spectrum, and up to the optical region.

The IEEE Transactions on Microwave Theory and Techniques invites manuscript submissions for a Special issue, with the aim to provide an appropriate venue, review perspectives, and foster innovations in the area of RF nanoelectronics/nanotechnology that is of interest for the MTT engineering community. Topics to be covered include, but are not limited to:

Devices and Systems:

- Carbon nanotubes (CNT), graphene and nanowire (NW) for RF electronics
- Graphene nanoribbon (GNR) circuits: transmission lines, discontinuities, and energy band filters
- Semiconductor- and other novel material-based nanotechnology for RF electronics
- Nano-structured microwave metamaterials
- Nano-wireless sensors and power meters
- Nano antennas and arrays
- THz nano-electronics/photonics (signal generation/processing, photo emission/detection/conversion)
- Nano- interconnects for advanced RF packaging
- Nanoscale electro-mechanical switches (NEMS) and resonators
- Spin waves for RF nano-electronics (spintronics) and molecular electronics
- Nano-particles and nano-plasmonic structures for RF applications
- Superconducting nanostructures and RF nanodevices for quantum information processing

First Special Issue will be published in IEEE Trans. MTT

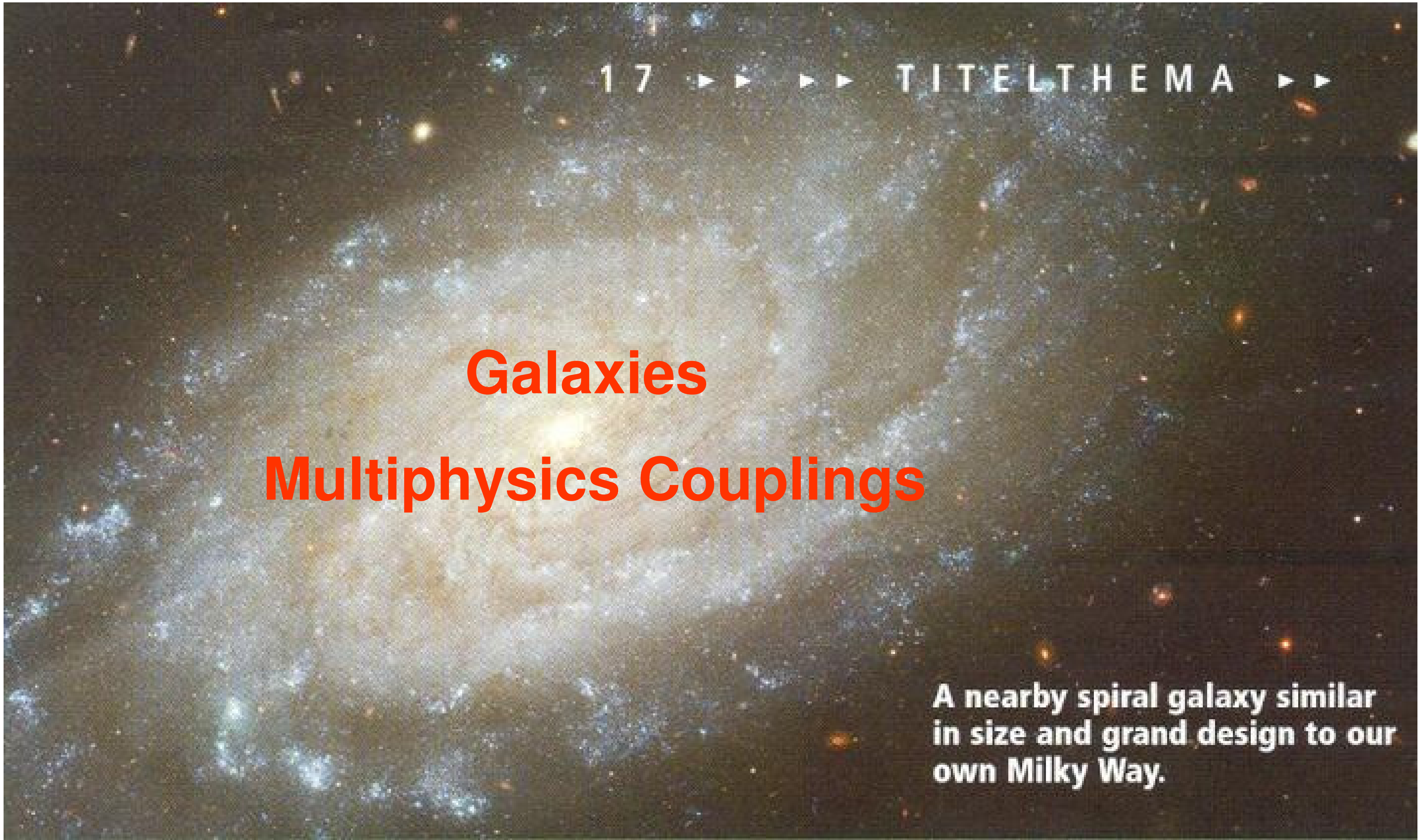
Theoretical Issues and Modeling:

- Multiphysics modeling of nanostructures and nano-devices
- Ballistic transport, periodic modes, wave solutions and multiport circuits in nano-materials
- Advanced techniques for the combined electromagnetic/coherent-transport problem in nano-devices
- Electrodynamics, field emission, radiation, detection and photo-generation in nano-structures
- Wave mixing, dispersive- and non linear-effects in nano-materials

Technology, Instrumentation, Imaging and Reliability

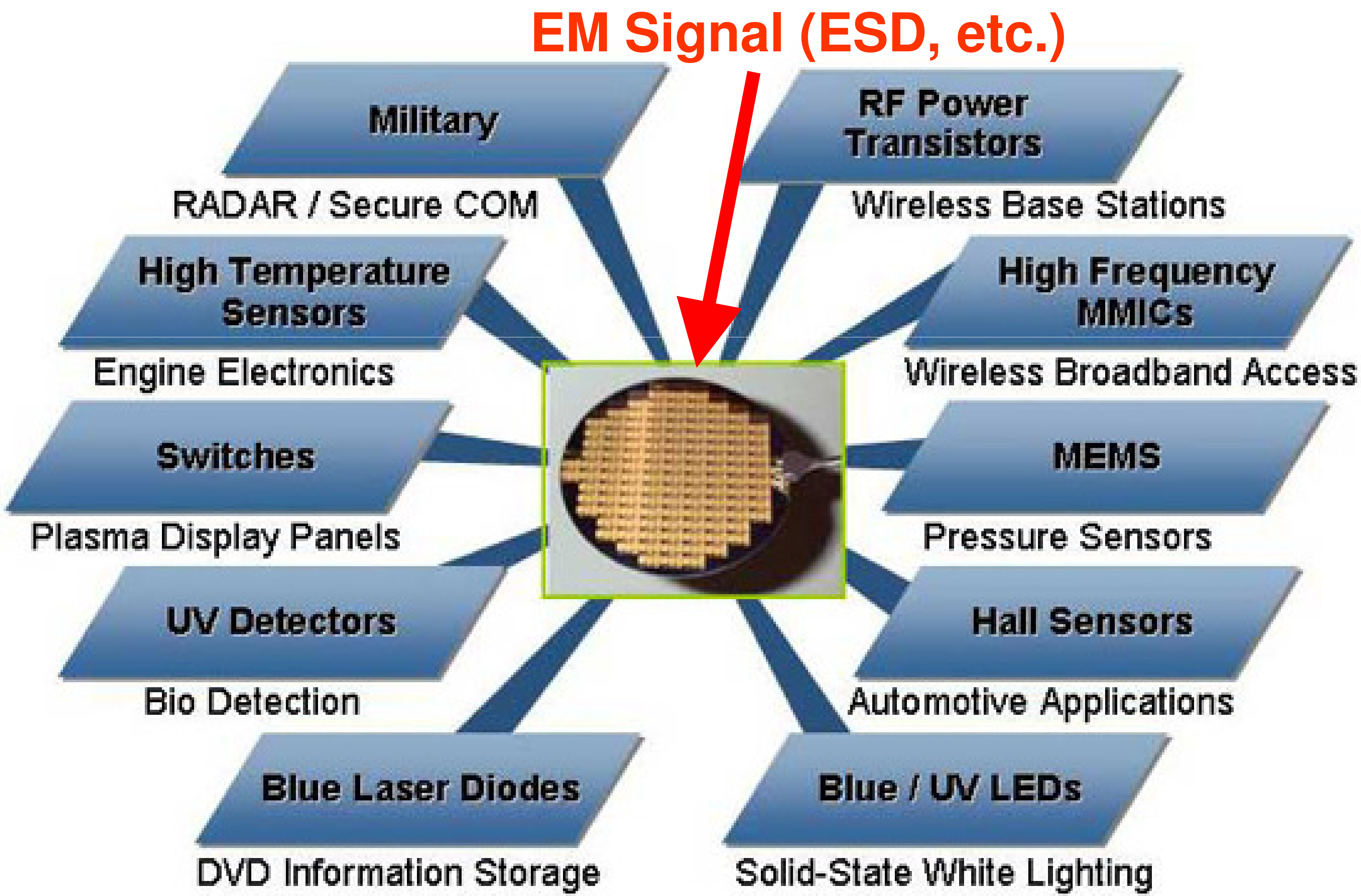
- Metrology and broadband characterization and of nanoscale devices/systems for RF applications
- Microwave nanoscale near field imaging and surface patterning
- Noise measurements of nanoscale devices
- CMOS compatibility and 3D-integration of carbon- and silicon/semiconductor-based nanodevices

Real World: Multiphysics

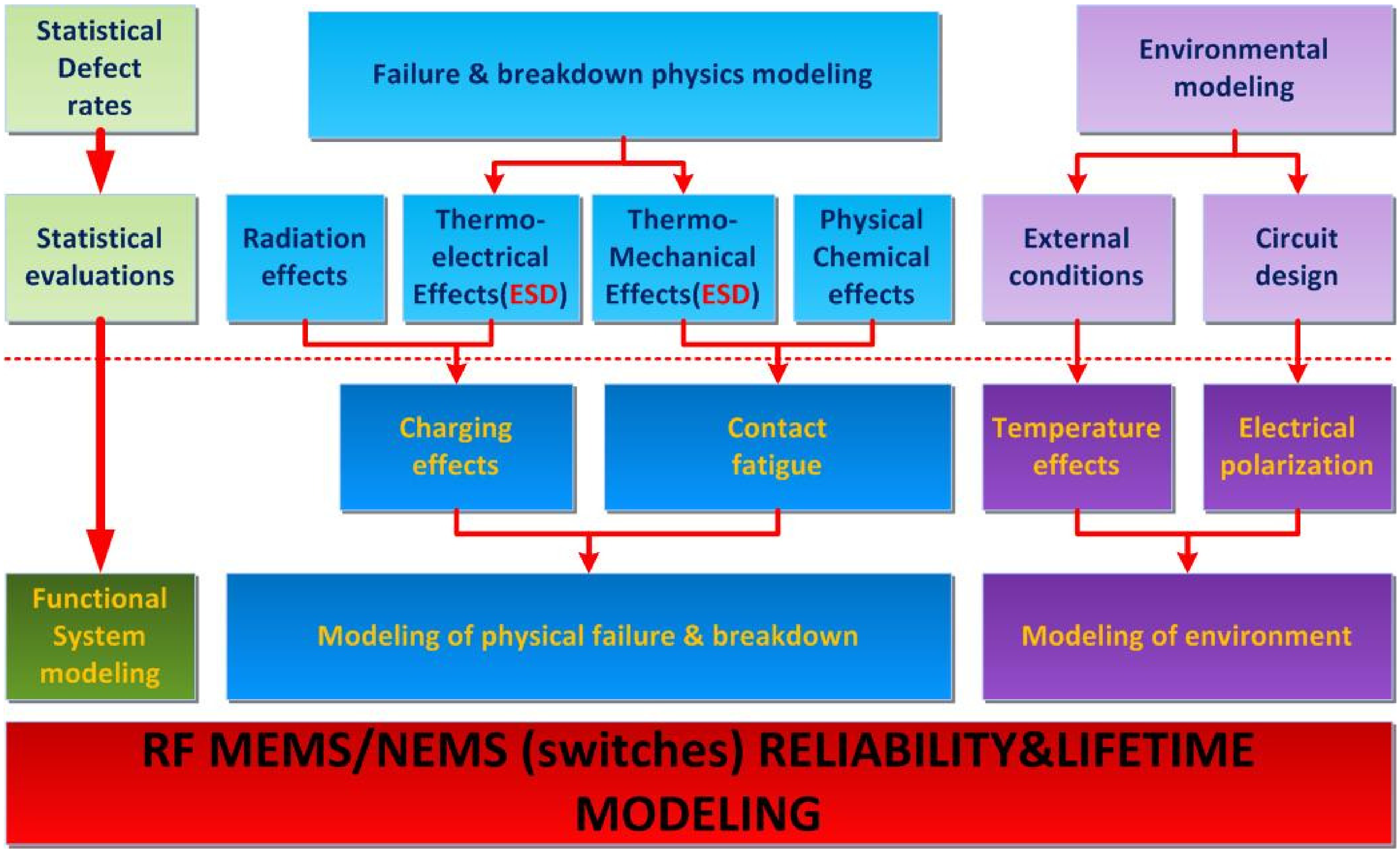


Global Thermal Effects

Multiphysics: Create So Many Chances

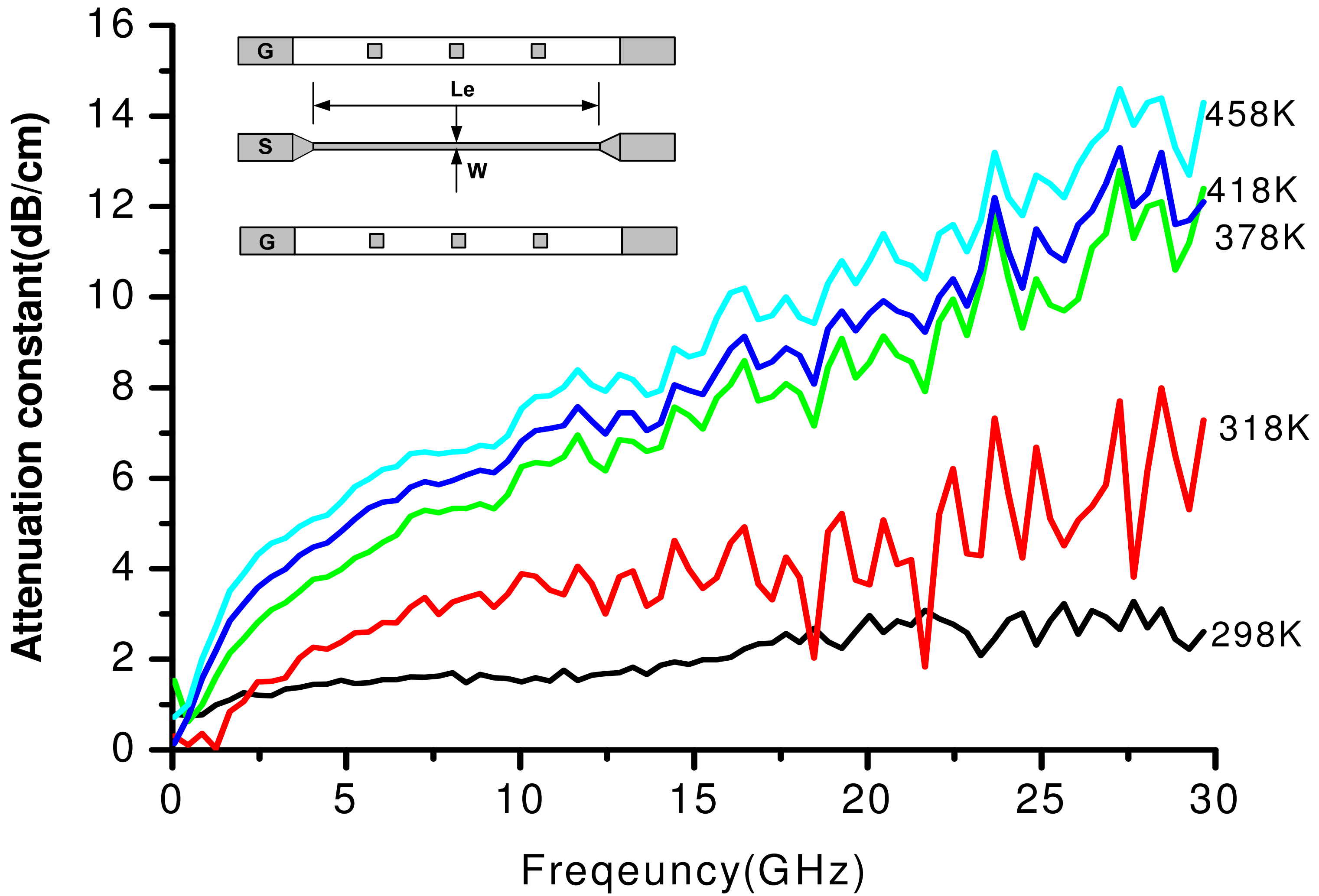


We Always Need Physical Compatibilities



Silicon-based Transmission Lines

Electrothermal Effects



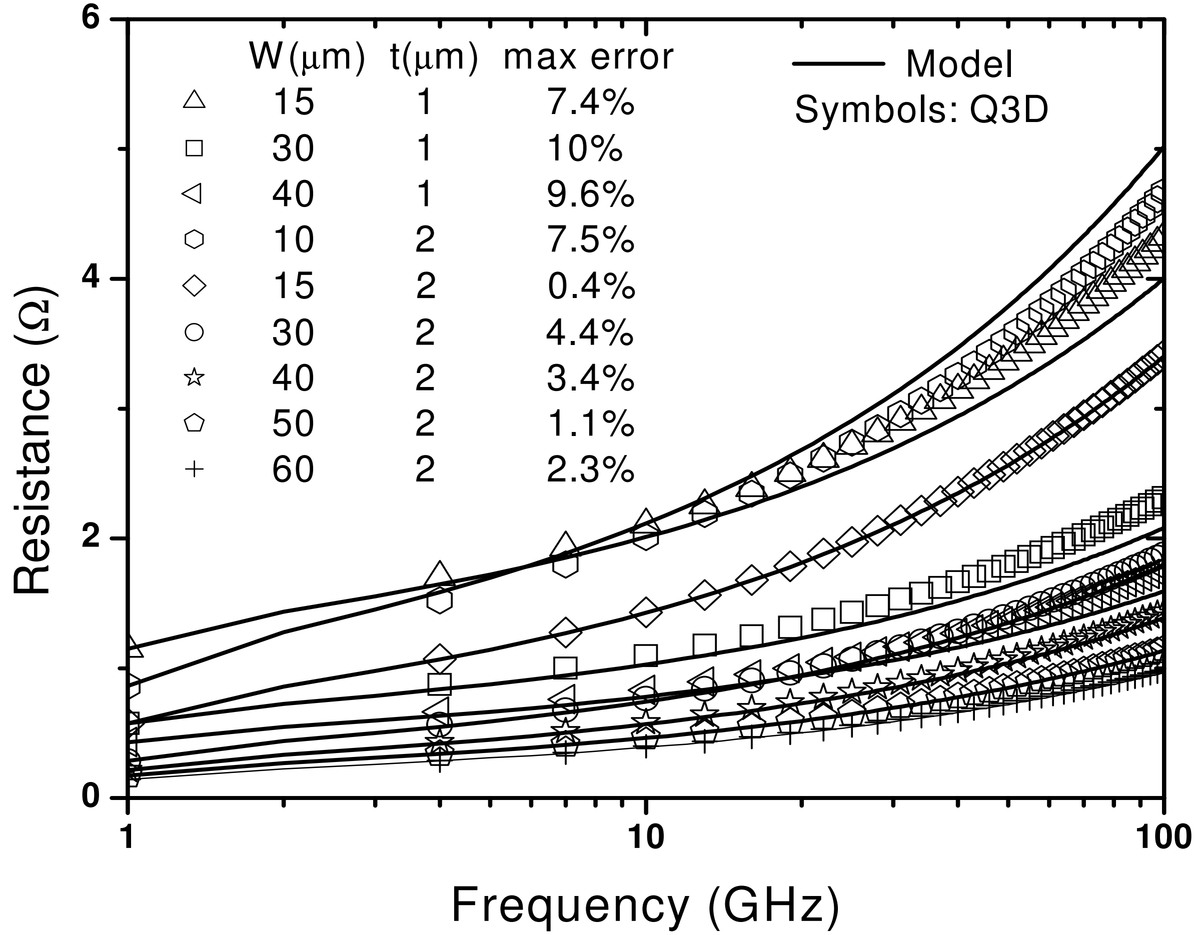
Finite electrical conductivity and semiconducting substrate!

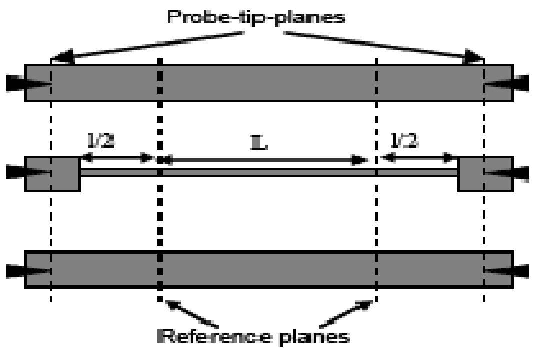
Problems

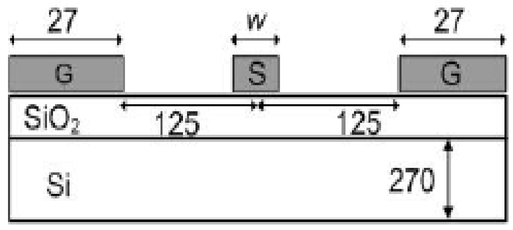
(1) **Temperature effects on electrical conductivities of most metal materials?**

(2) **Temperature effects on thermal conductivities of most semiconducting materials?**

Silicon-based Millimeter Wave TLs

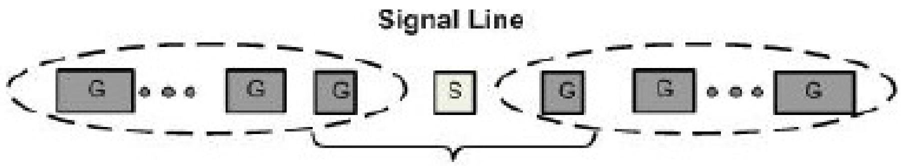


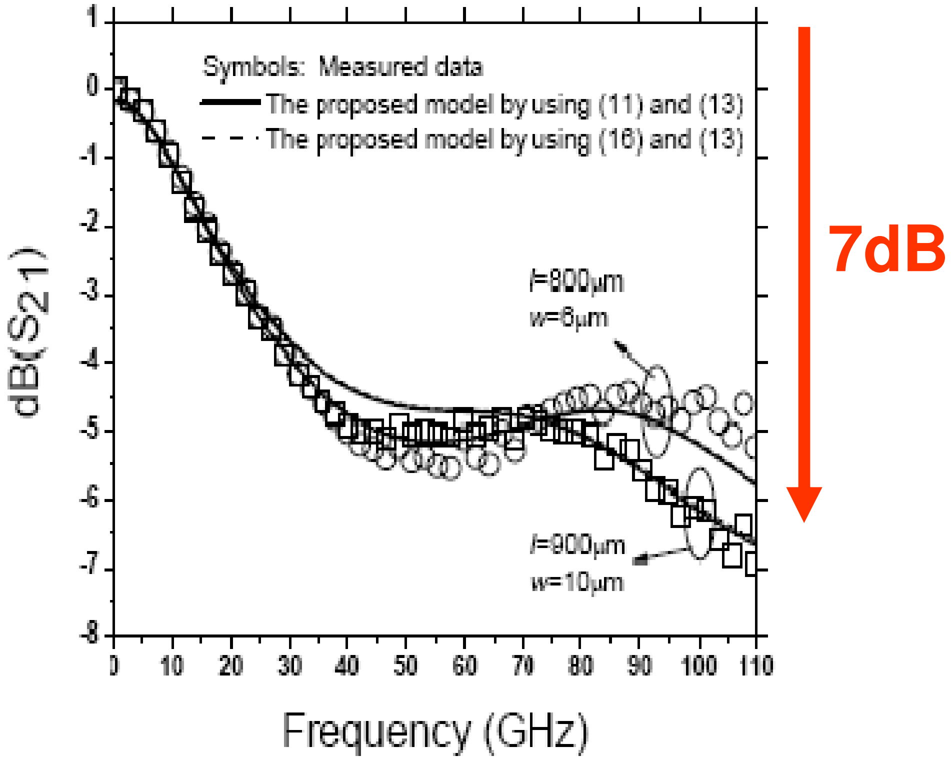


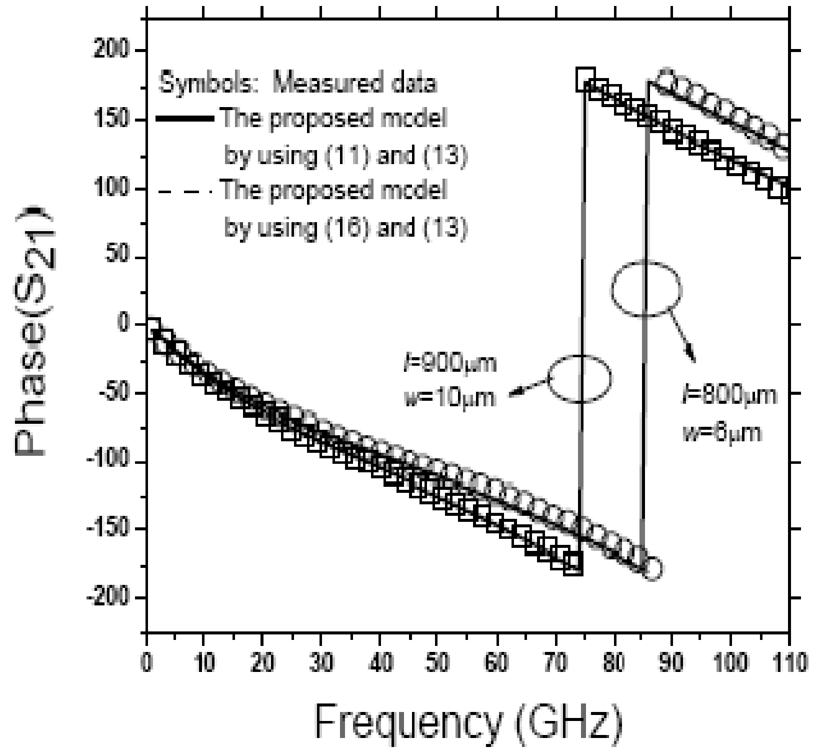


K. Kang, L. Nan, S. C. Rustagi, W. Y. Yin, et al, "A wideband scalable and SPICE-compatible model for on-chip interconnects up to 110 GHz," IEEE Trans. Microwave Theory Tech., 56(4), 942-951, 2008.

Silicon-based Millimeter Wave TLs





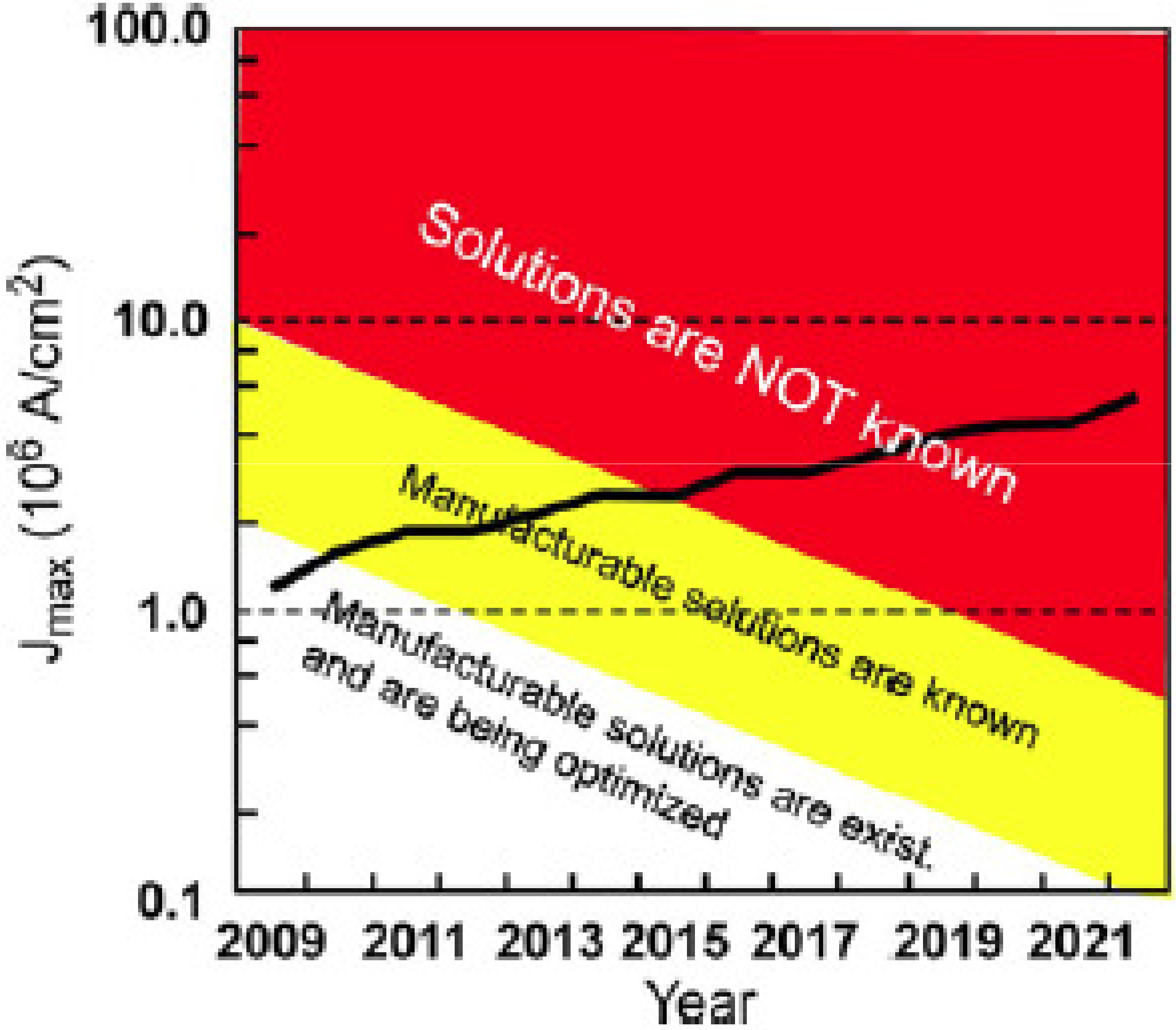


ITRS

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal levels	13	13	13	14	14	14	14
Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	3571	4000	4545	5000	5555	6250	7143
FITs/m length/$cm^2 \times 10^{-3}$ excluding global levels [2]	1.4	1.3	1.1	1	0.9	0.8	0.7
J_{max} (A/cm^2) – intermediate wire (at 105°C)	1.06E+07	1.14E+07	1.47E+07	1.54E+07	1.80E+07	2.23E+07	2.74E+07
Metal 1 wiring pitch (nm)	56	50	44	40	36	32	28
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	5.2	5.58	6.01	6.33	6.7	7.34	8.19

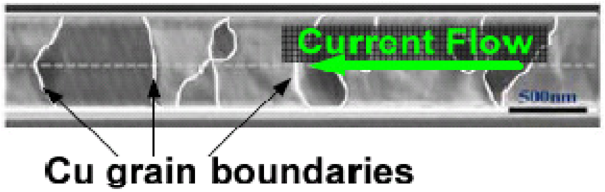
After 2014: $J_{max} > 1.06 \times 10^7$ A/cm2

Final Solutions are not Known

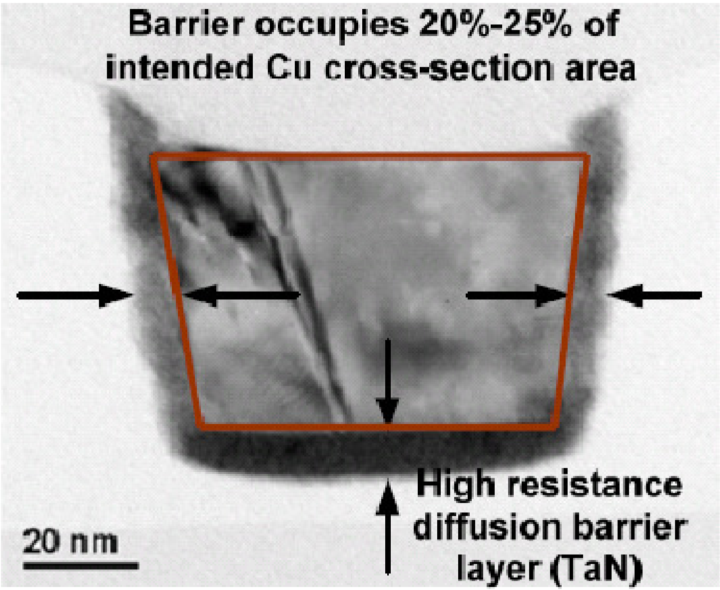


Y. Awano, et al., PIEEE, 98(12), 2015-2031, 2010.

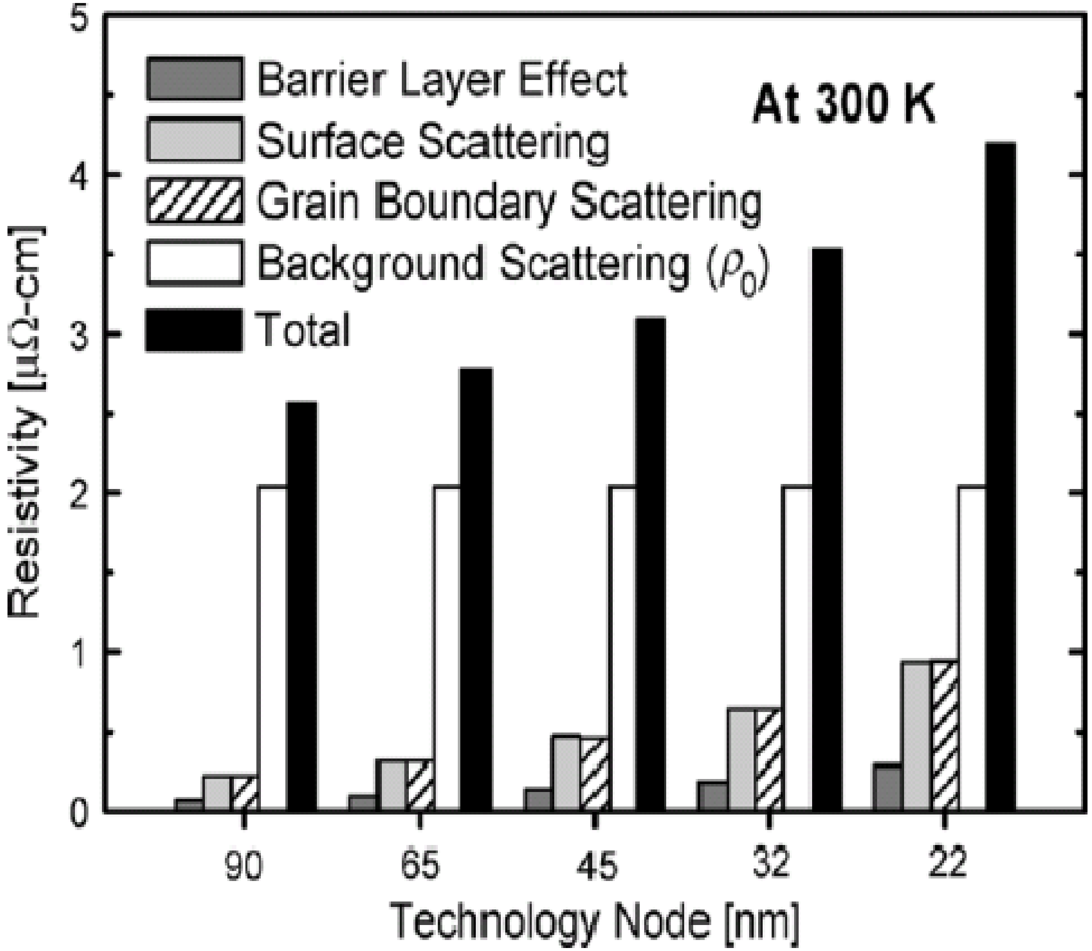
Size Effect in Cu Interconnect



Top-view TEM of Cu interconnect



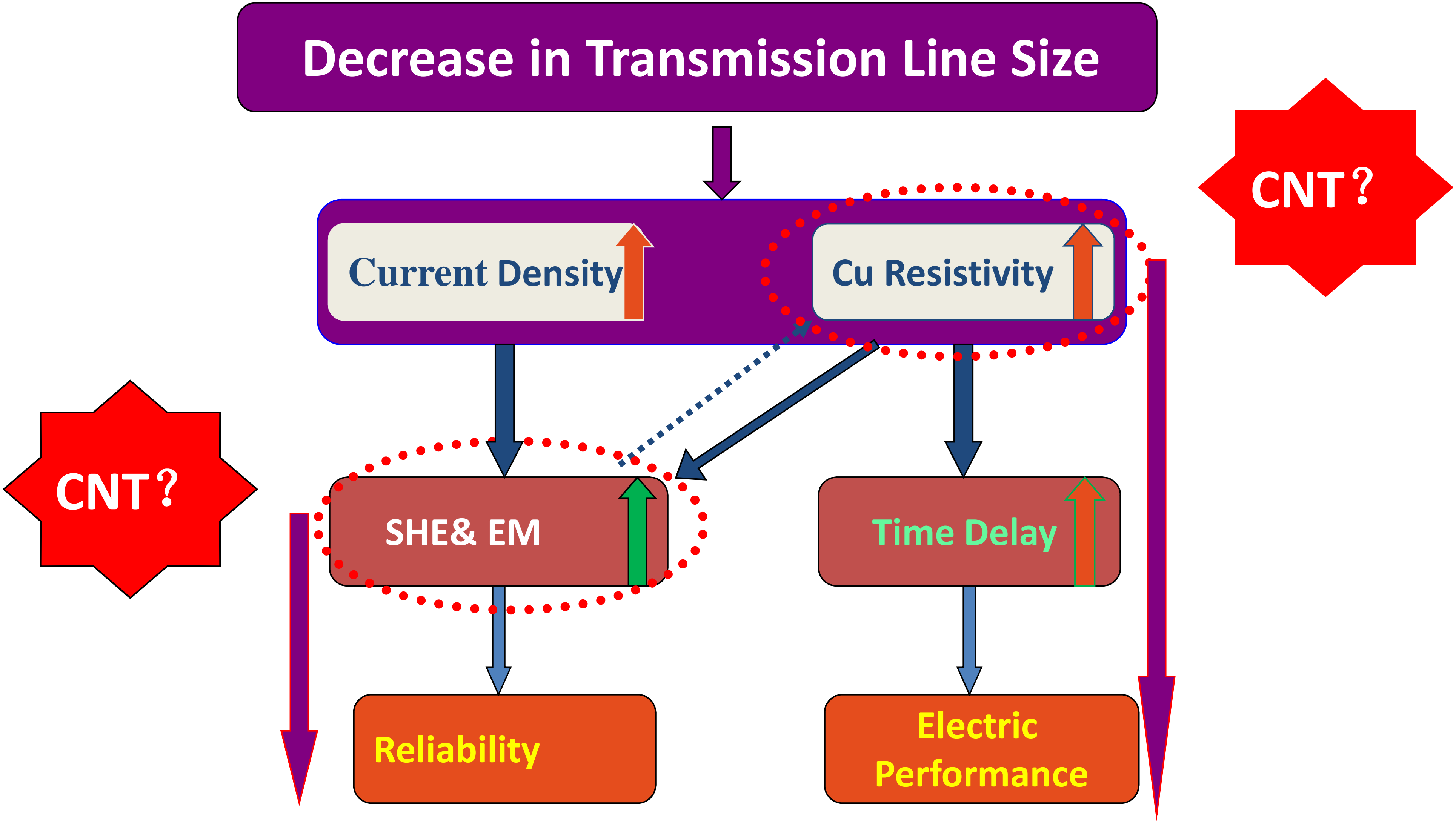
TEM cross-section of narrow Cu interconnect



Cu resistivity will be increased rapidly!
Electric performance and reliability will be decreased due to self-heating effect !

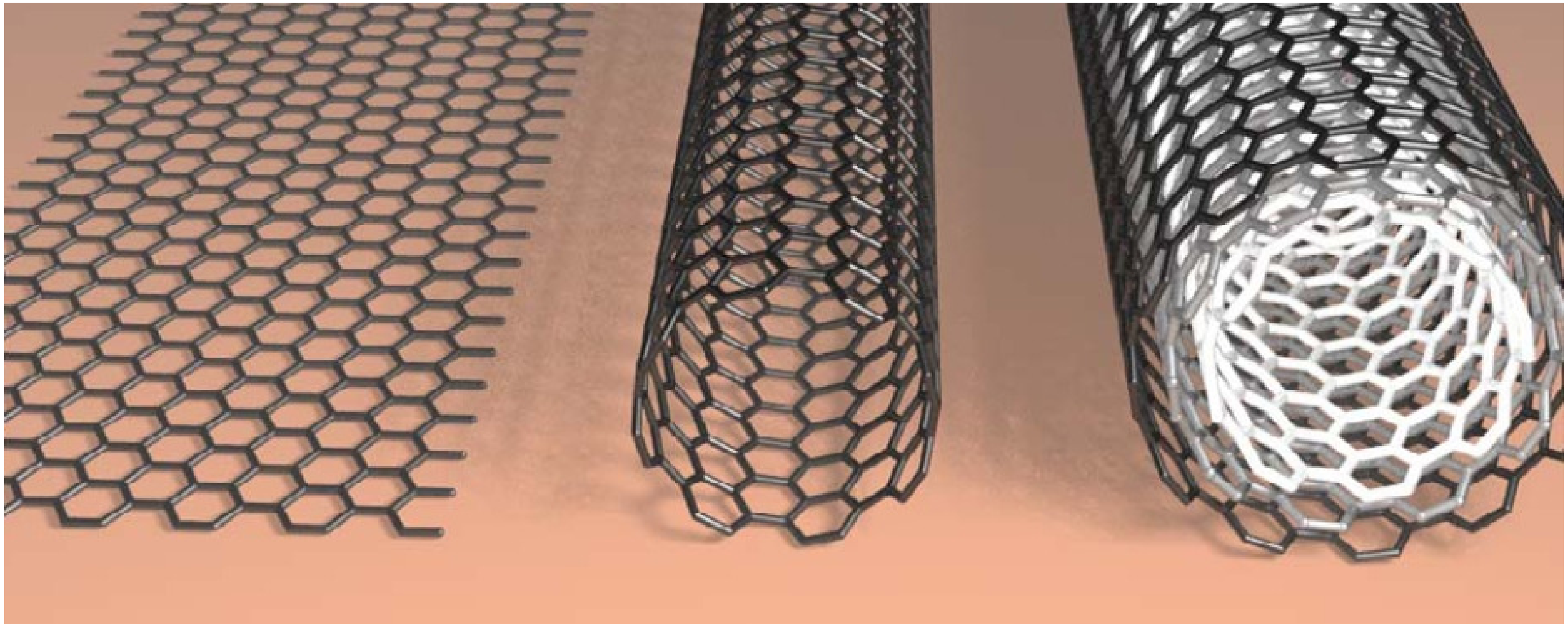
Steinhogl *et al.*, *JAP*, 2005

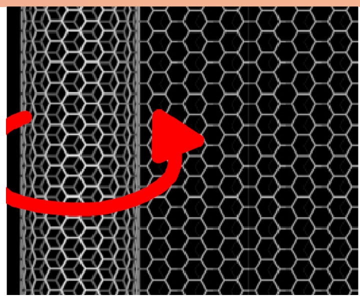
CNT Solution



Carbon Nanotube Transmission Lines (CNTL): Beyond Maxwell's Equations

CNT



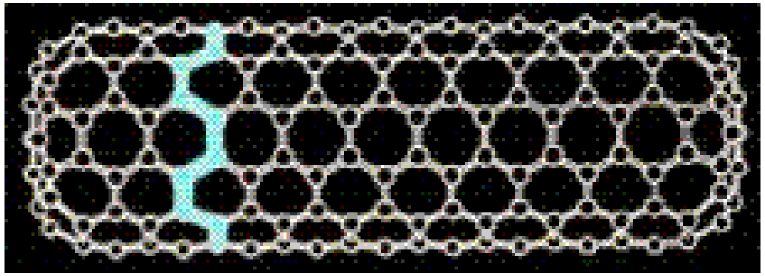


GR SWCNT MWCNT

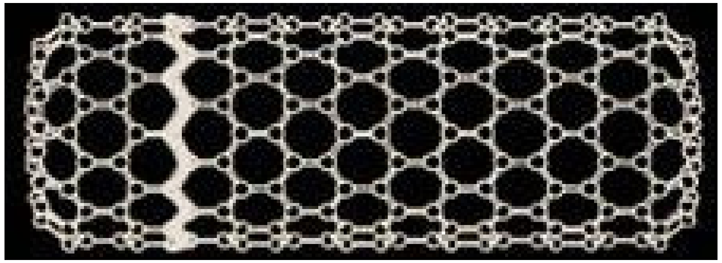
Courtesy: F. Kreupl, Infineon

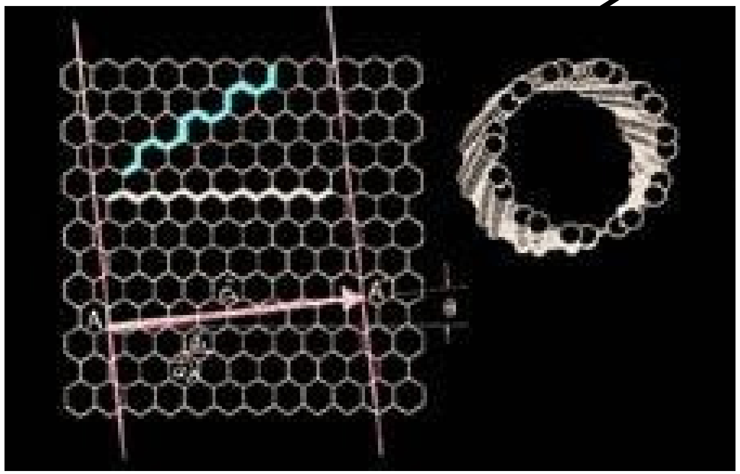
CNT Classification

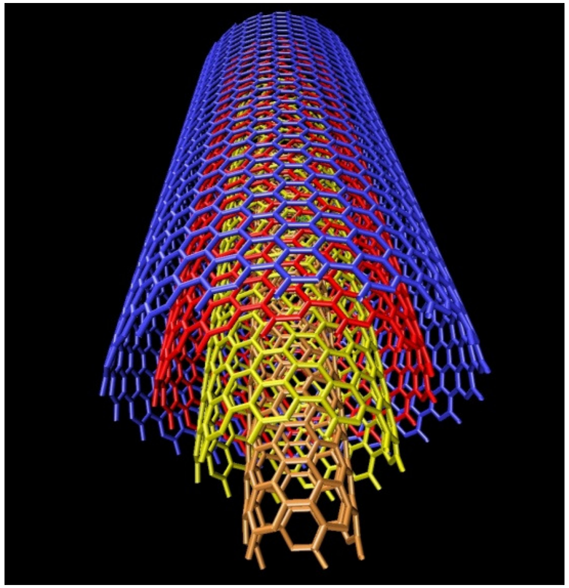
Arm-Chair CNT(M)



Zig-Zag CNT (M & S)







MWCNT
(each wall can be S or M, most walls are M)

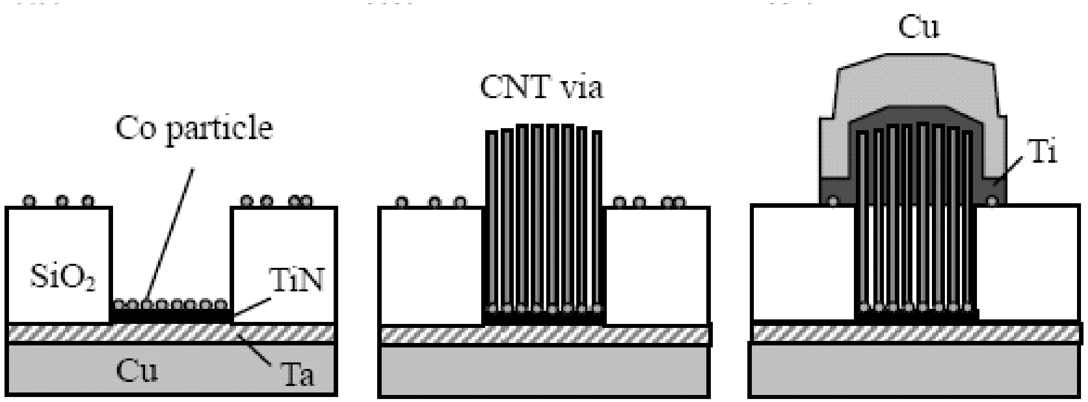
About 1/3 of all SWCNTs are metallic and 2/3 are semiconducting

Metallic SWCNT Properties

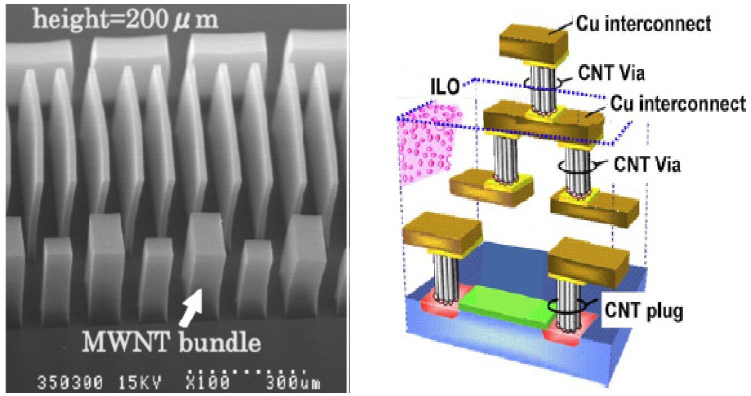
- **Length: um-mm**
- **Diameter: 0.4-100nm**
- **Strength : 45 Tpa! (Steel ~ 2Tpa)**
- **Thermal stability: operating temperature up to 700 º C.**

	CNT	Cu
Maximum current carrying density(A/cm*cm)	$>1X10^9$ Radosavljevic, et al., *Phys. Rev. B*, 2001	$<1X10^7$
Thermal conductivity (W/mK)	5800 Hone, et al., *Phys. Rev. B*, 1999	385
Mean free path（diameter=1nm）	>1000 McEuen, et al., *IEEE Trans. Nano.*, 2002	40

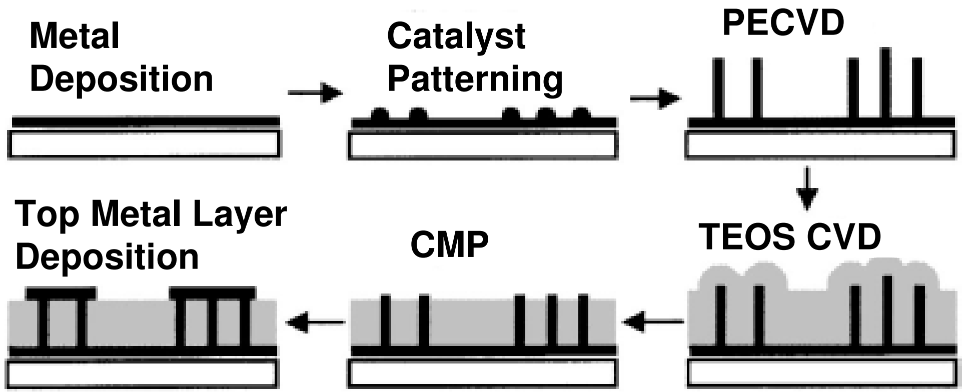
CNT Vias



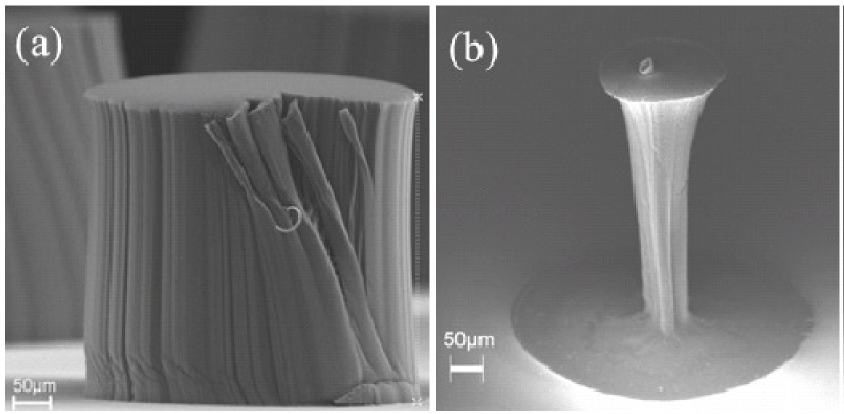
The growth of carbon nanotube interconnect technology
S. Sato et al., *IITC*, 2006.



Vertical array of multi-walled carbon nanotube bundles
Y. Awano, *IEICE TE*, 2006; PIEEE, 2010.

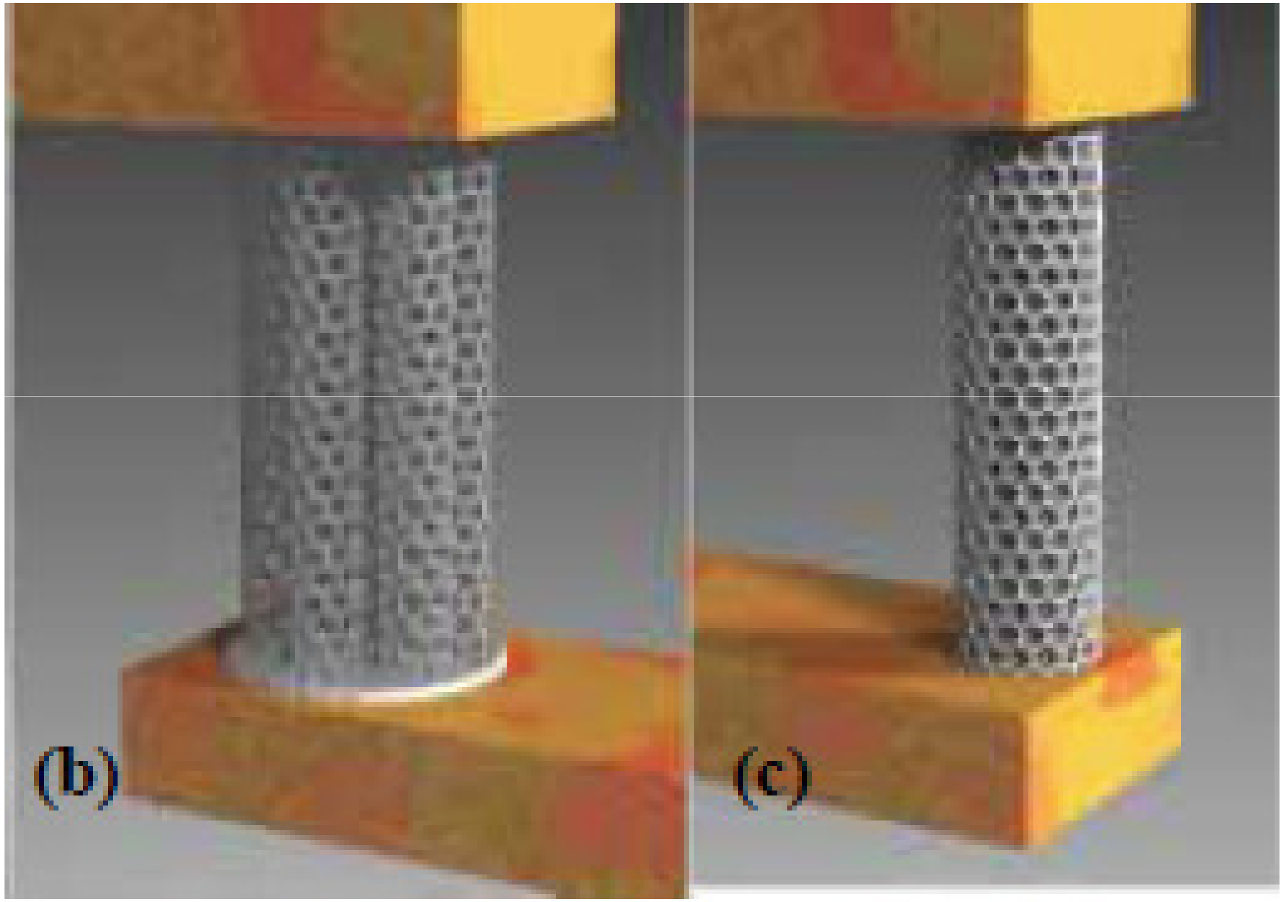


A bottom-up growth of carbon nanotube interconnect technology
J. Li et al., *APL*, 2003.



High density of carbon nanotube bundles
Z. Liu, et al., *IITC*, 2007.

CNT Vias



Carbon Nanotubes for Interconnect Applications

Franz Kreupl, Andrew P. Graham, Maik Liebau, Georg S. Duesberg, Robert Seidel, Eugen Unger
Infineon Technologies AG, Corporate Research, Otto-Hahn-Ring 6, 81739 Munich, Germany
Tel: +498923444618, email: franz.kreupl@infineon.com

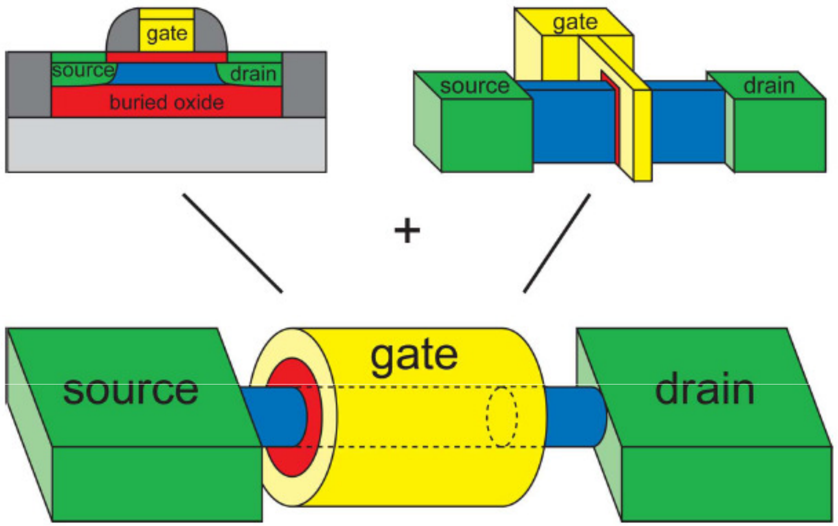
Carbon Nanotubes for Active Nano Devices

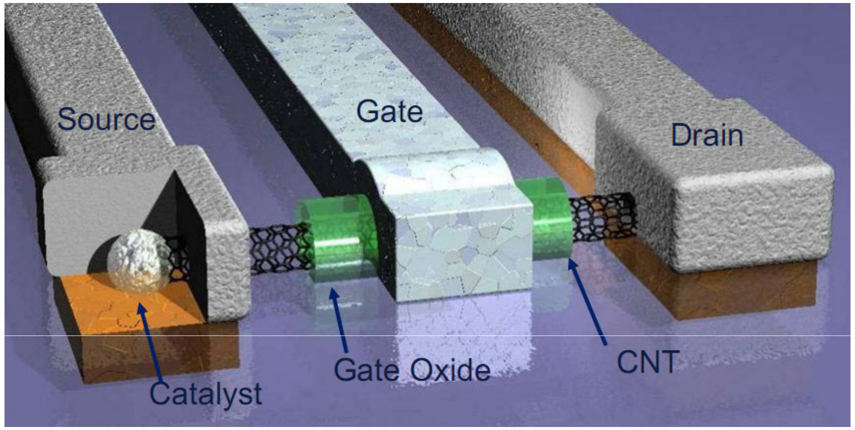
Semiconducting SWCNT Properties

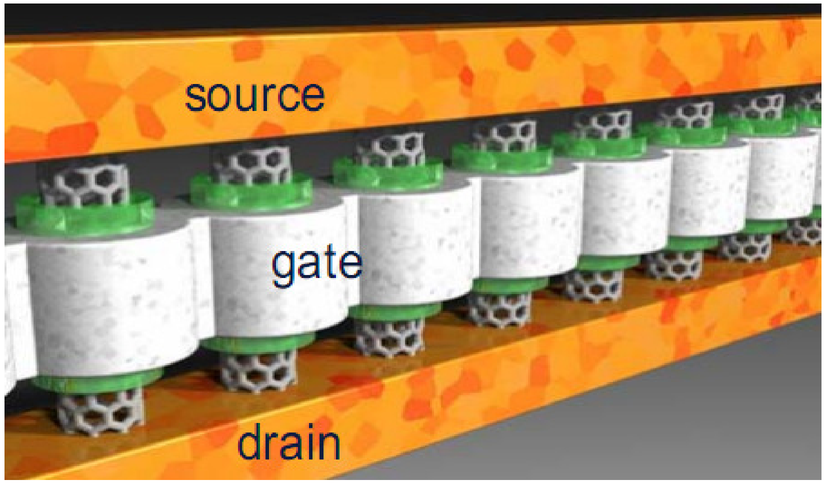
Comparison of CNT properties with other semiconductors.

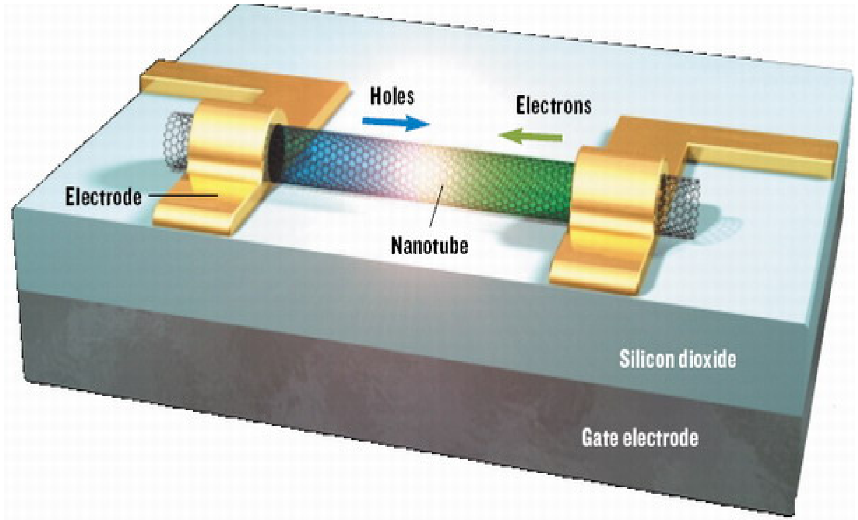
	Bandgap (eV)	Electron Mobility (cm^2/Vs)	Saturated Electron Velocity (107cm/s)	Thermal Conductivity (W/cm-K)
CNT	~0.9	100,000	>10	>30
InAs	0.36	33,000	0.04	0.27
Si	1.1	1,500	0.3	1.5
GaAs	1.42	8,500	0.4	0.5
InP	1.35	5,400	0.5	0.7
4HSiC	3.26	700	2.0	4.5
GaN	3.49	900	3.3	20

CNTFETs

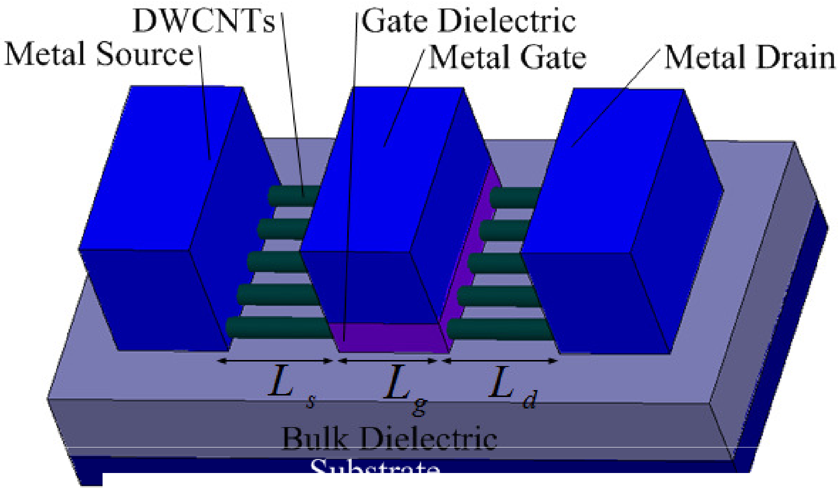

gate
source
drain
buried oxide
gate
source
drain
+
gate
source
drain

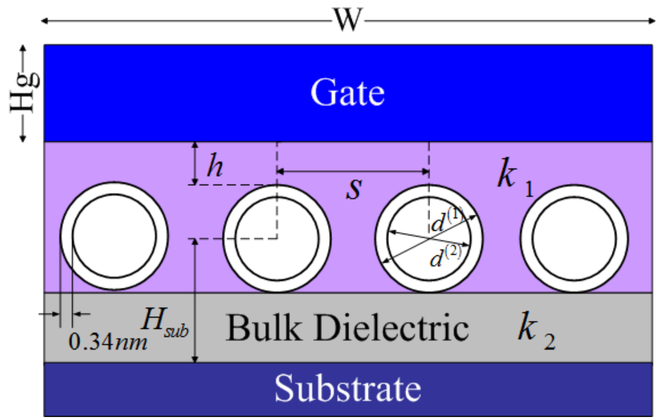

Source
Gate
Drain
Catalyst
Gate Oxide
CNT

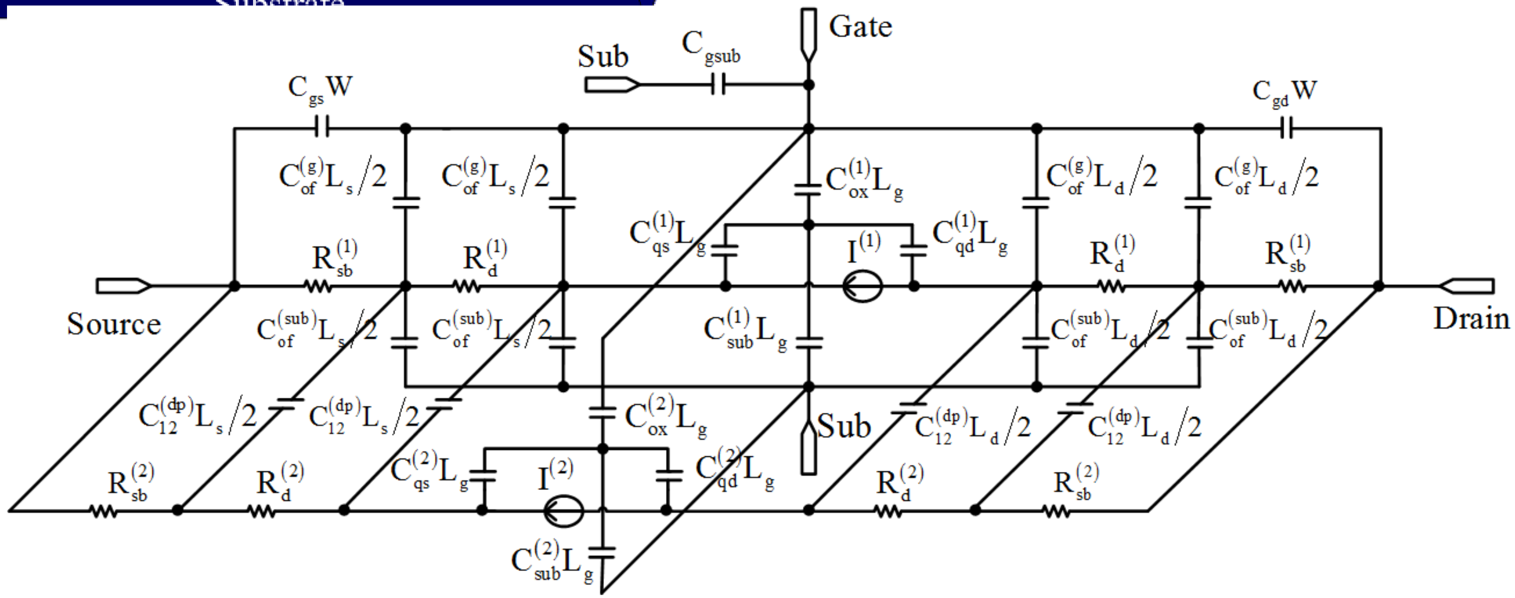

source
gate
drain


Holes
Electrons
Electrode
Nanotube
Silicon dioxide
Gate electrode

DWCNTFETs

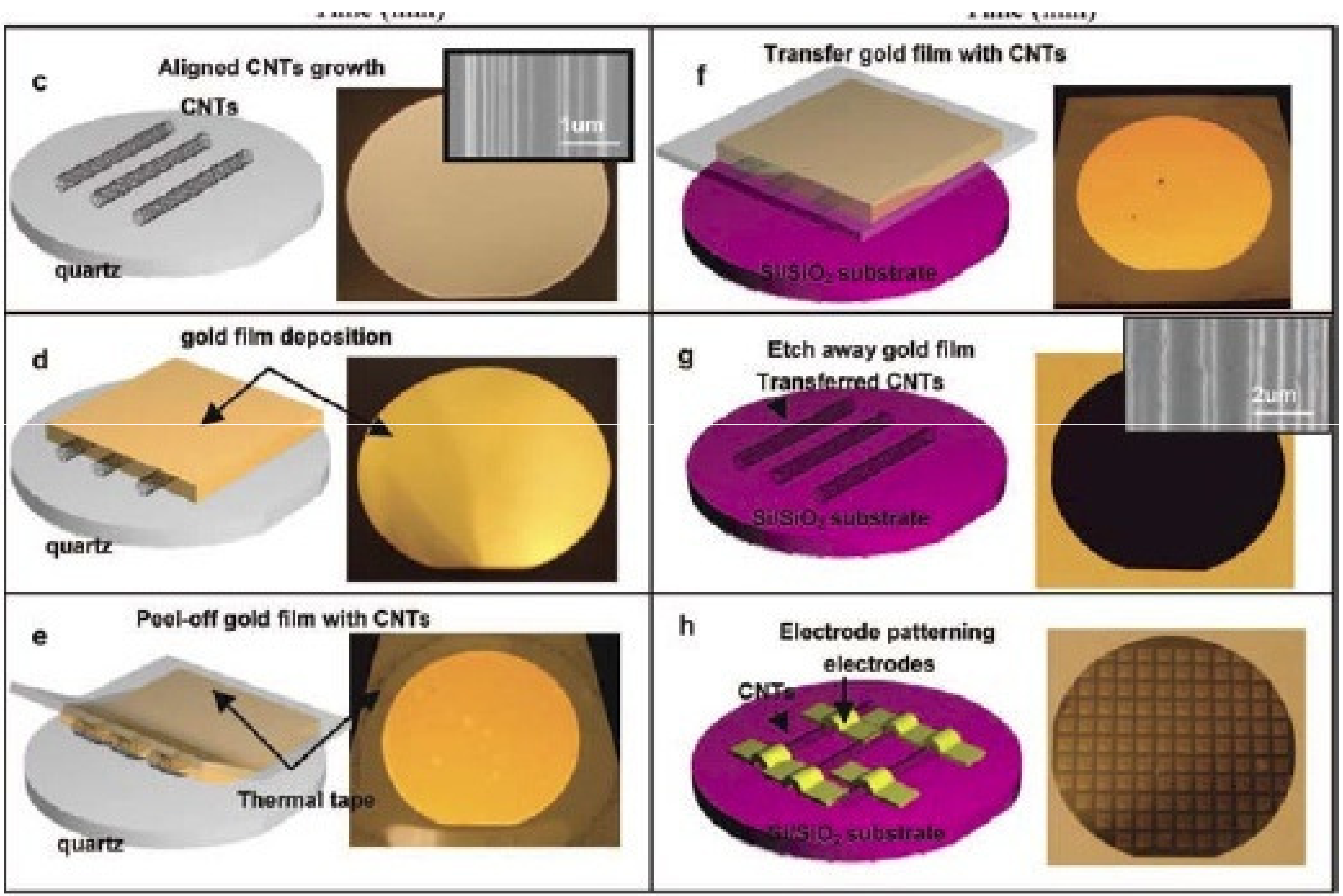






J. Huang and Wen-Yan Yin, *IEEE Trans. Electronic Devices*, 58(1), 2011.

Fabrication



K. Ryu, and H.S.P. Wong, *et al*., *Nano Lett*., 9(1), 189-197, 2009.

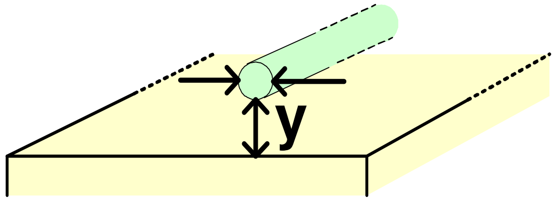
Electromagnetic Capability-Oriented Study on CNTLs

Multiphysics Issues:

Beyond Maxwell's Equations: Quantum Effects

Both Frequency- and Temperature-Dependent

Distributed Parameters of a SWCNT

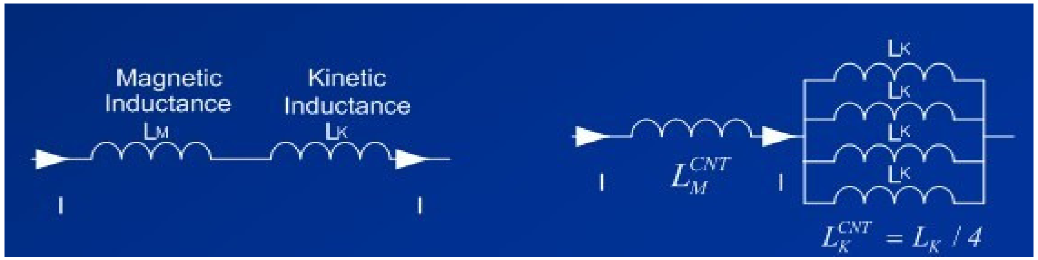


Kinetic Inductance

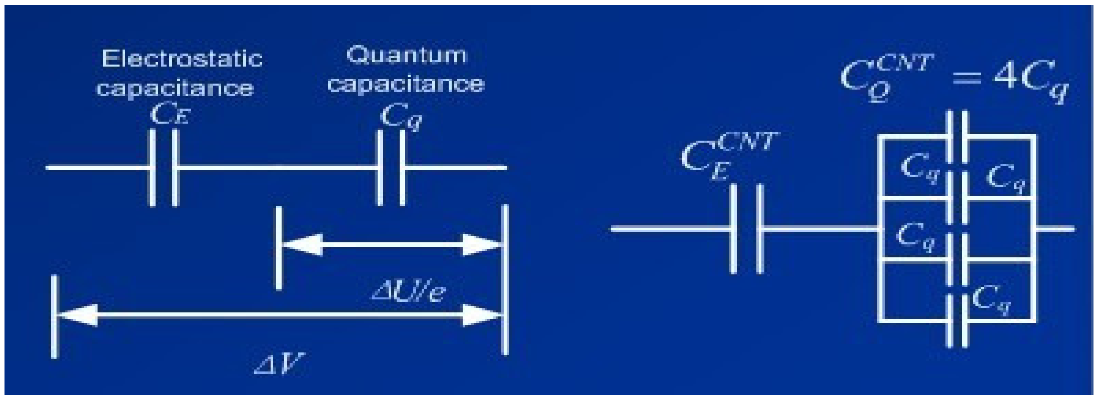
$$L_{k-CNT} = \frac{h}{2 v_F e^2}$$

$$L_K \approx 16 nH / \mu m$$

$$L_M^{CNT} = \frac{\mu}{2\pi} \ln\left(\frac{y}{d}\right)$$



Quantum Capacitance

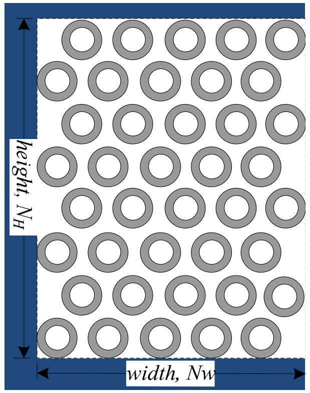


$$C_Q = \frac{\Delta Q}{\Delta V} \sim 96 aF / \mu m$$

$$C_E = \frac{2\pi\varepsilon}{\ln(2h/d)}$$

SWCNT Bundle

$$R_{CNT} = R_C + R_Q\left(1 + \frac{\ell_{CNT}}{\ell_{mfp}}\right)$$
$$= (R_C + R_Q) + \frac{R_Q}{\ell_{mfp}}\ell_{CNT}$$
$$= R_l + R_d \ell_{CNT};$$



Quantum Resistance

$$R_Q = 6.45K\Omega$$

Contact Resistance

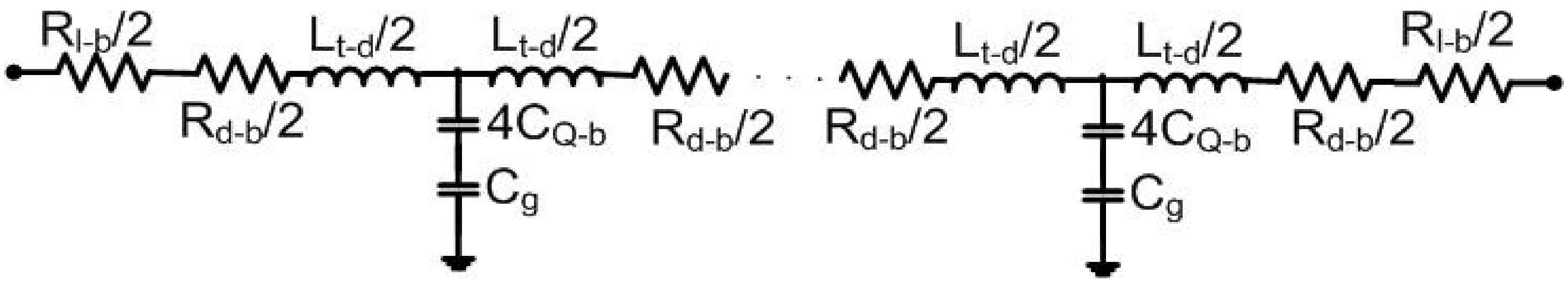
$$R_C$$

$$C_{Q-b} = C_Q \cdot n_{CNT}$$

$$L_{k-b} = \frac{L_{k-CNT}}{4n_{CNT}}$$

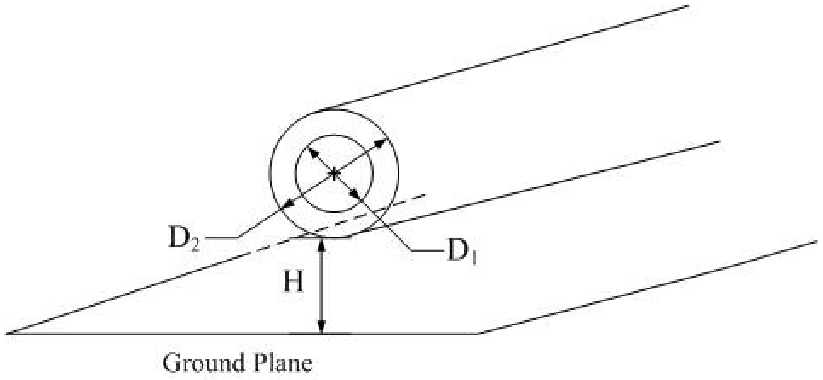
$$R_b = \frac{R_{CNT}}{n_{CNT}} = \frac{(R_C + R_Q)}{n_{CNT}} + \frac{R_Q}{n_{CNT}\ell_{mfp}}\ell_{CNT} = R_{lb} + R_{db}\ell_{CNT};$$

$$L_t = \frac{L_{k-b} + L_{M-b}}{\ell_{CNT}} \cdot \ell_{CNT} = L_{t-d} \cdot \ell_{CNT}.$$



Equivalent circuit model of a SWCNT bundle

DWCNT



$$C_{CM} = \frac{2\pi\varepsilon}{\ln(D_2 / D_1)};$$

$$C_{CM-b} = C_{CM} \cdot n'_{CNT};$$

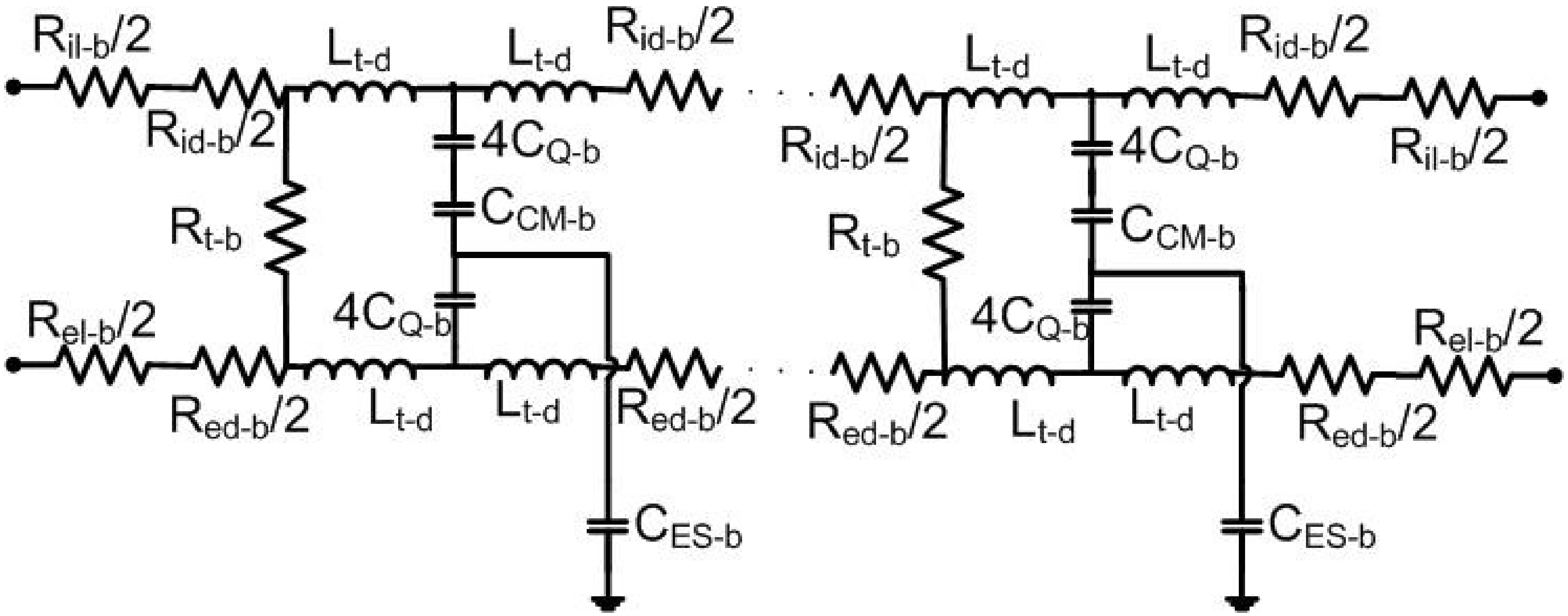
$$C_{ES-b} = C_{ESext} \cdot n'_{CNT};$$

$$C_{Q-b} = C_Q \cdot n'_{CNT}.$$

$$R_{i-b} = \frac{R_{\text{int}}}{n'_{CNT}} = \frac{(R_C + R_{Qi})}{n'_{CNT}} + \frac{R_{Qi}}{n'_{CNT}\,\ell_{mfpi}}\ell_{CNT} = R_{il-b} + R_{id-b}\ell_{CNT};$$

$$R_{e-b} = \frac{R_{ext}}{n'_{CNT}} = \frac{(R_C + R_{Qe})}{n'_{CNT}} + \frac{R_{Qe}}{n'_{CNT}\,\ell_{mfpe}}\ell_{CNT} = R_{el-b} + R_{ed-b}\ell_{CNT}.$$

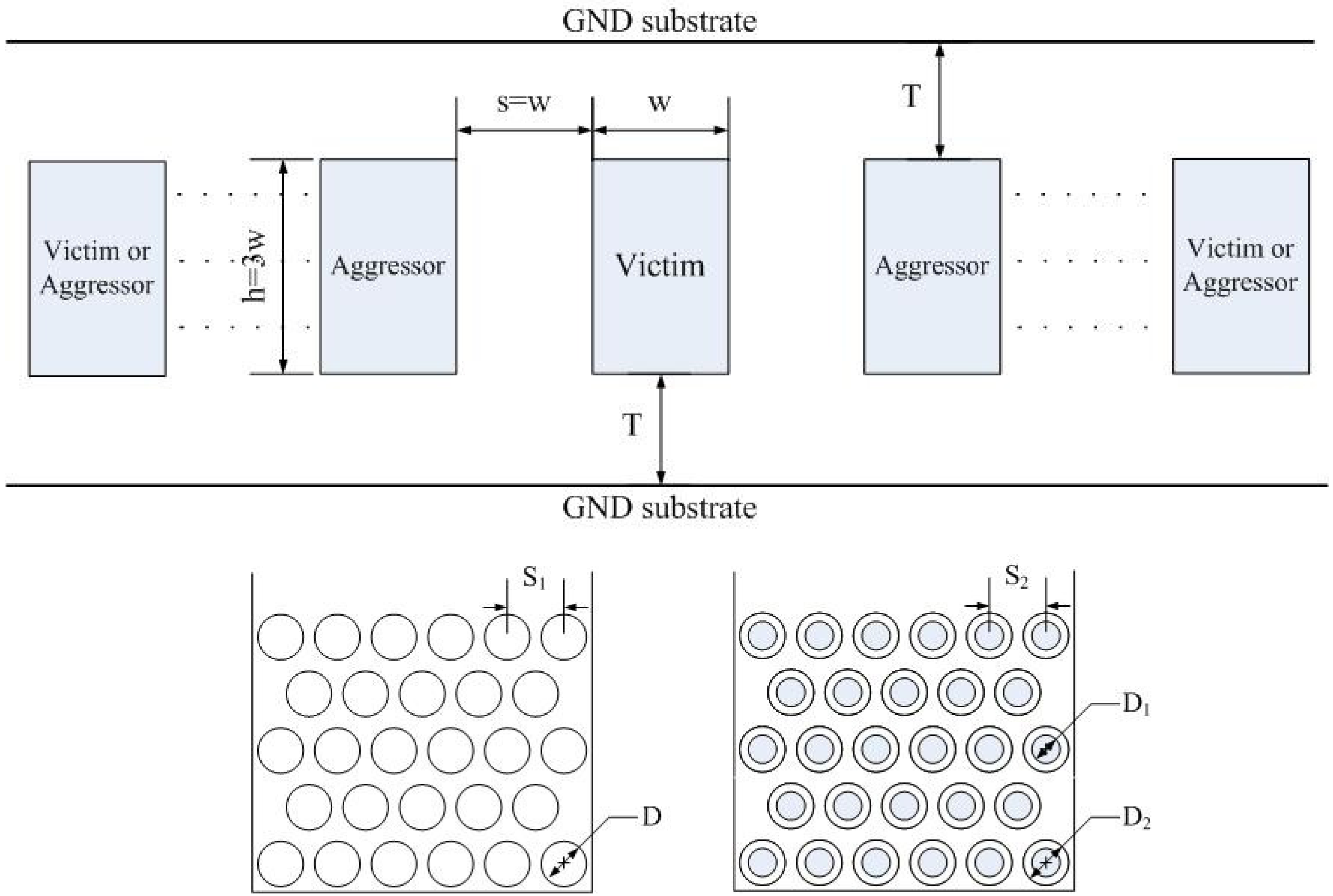
DWCNT Bundle



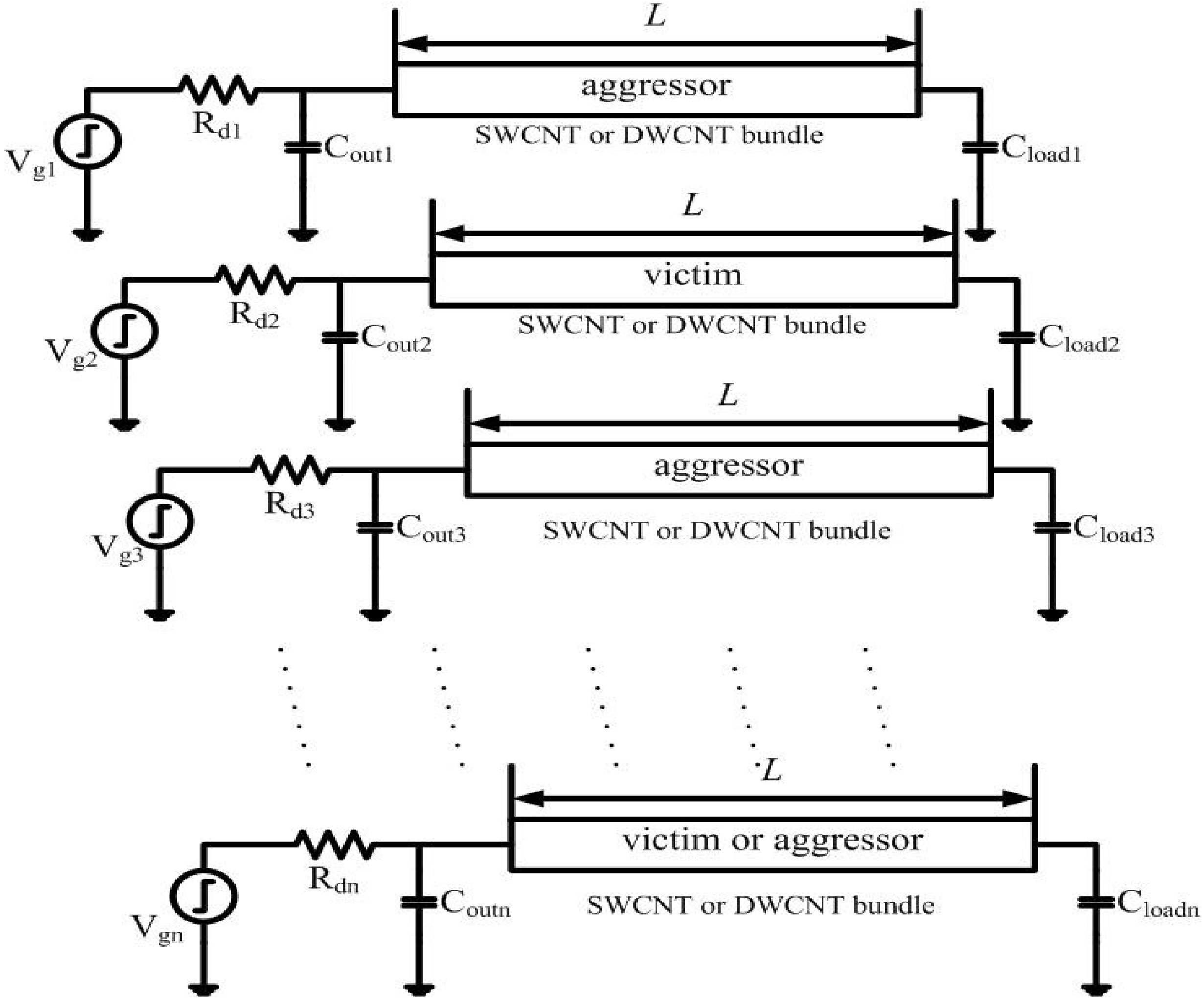
Equivalent circuit model of a DWCNT bundle

S. N. Pu, Wen-Yan Yin, J. F. Mao, *et al.* , "Crosstalk prediction of single and double-walled carbon nanotube(SWCNT/DWCNT) bundle interconnects," *IEEE Trans. Electron Devices*, 56(4), 560-568, 2009

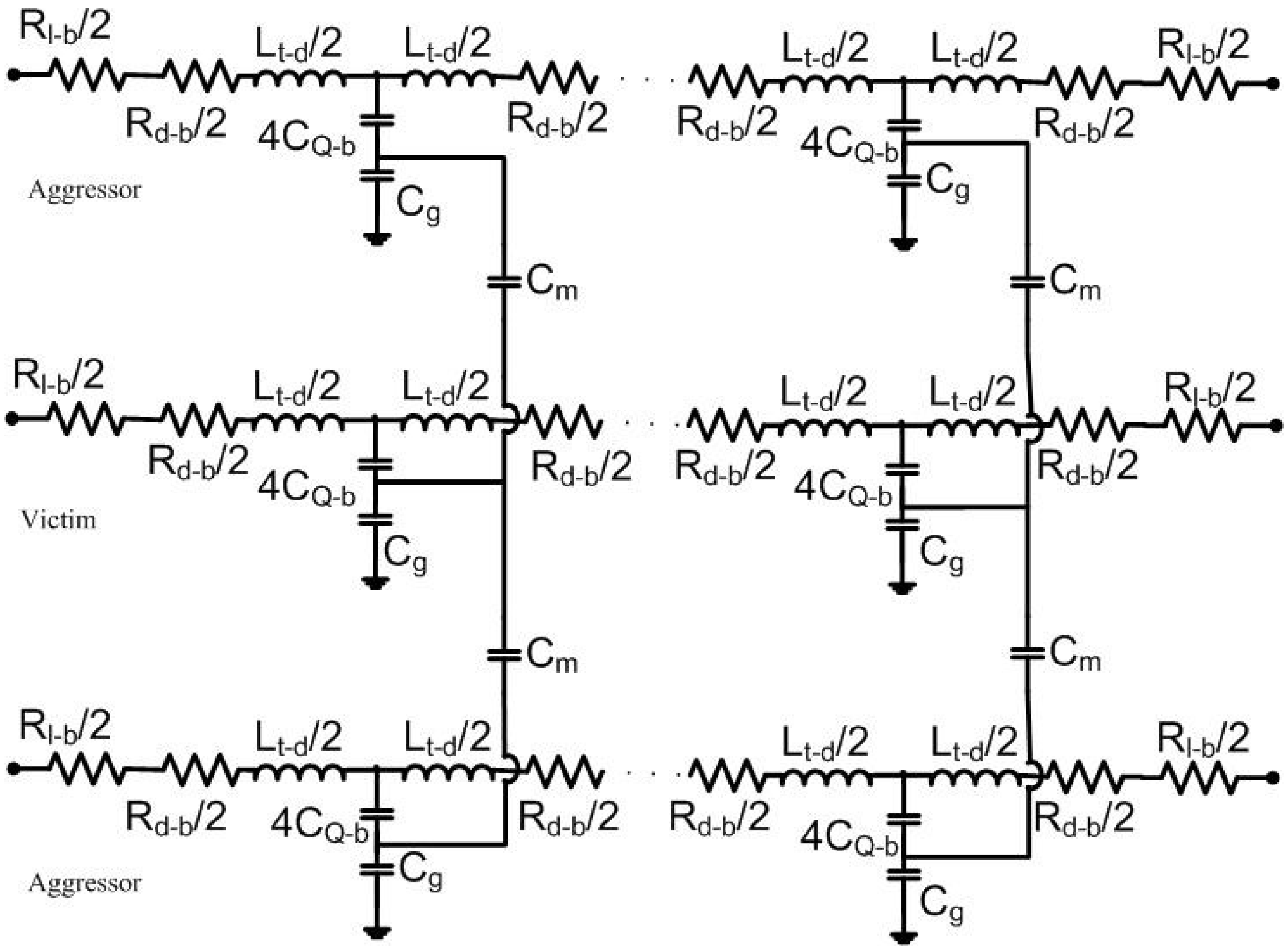
DWCNT Bundle TL



Multi-SWCNT/DWCNT Bundle TL

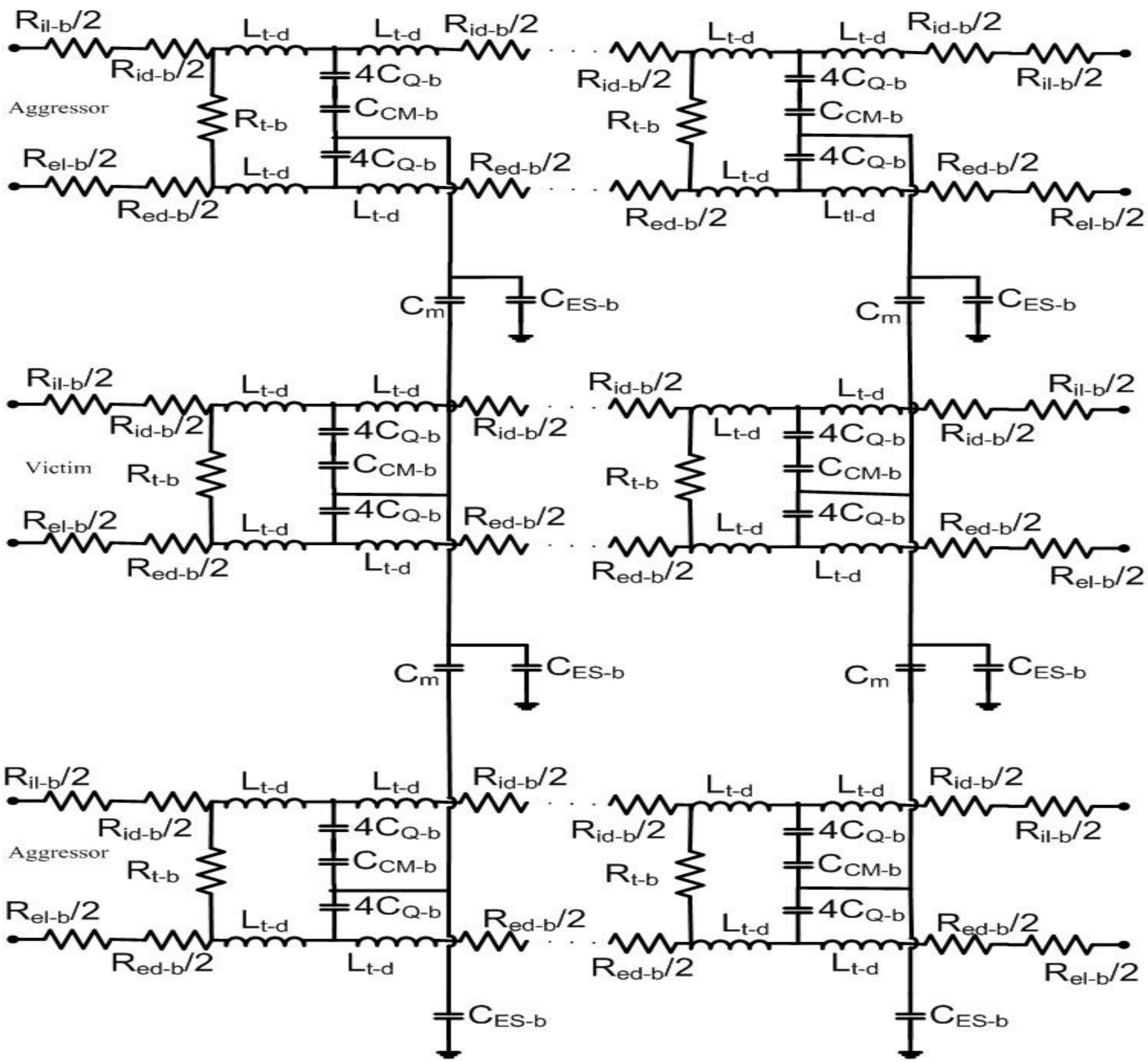


Tri-SWCNT Bundle TL



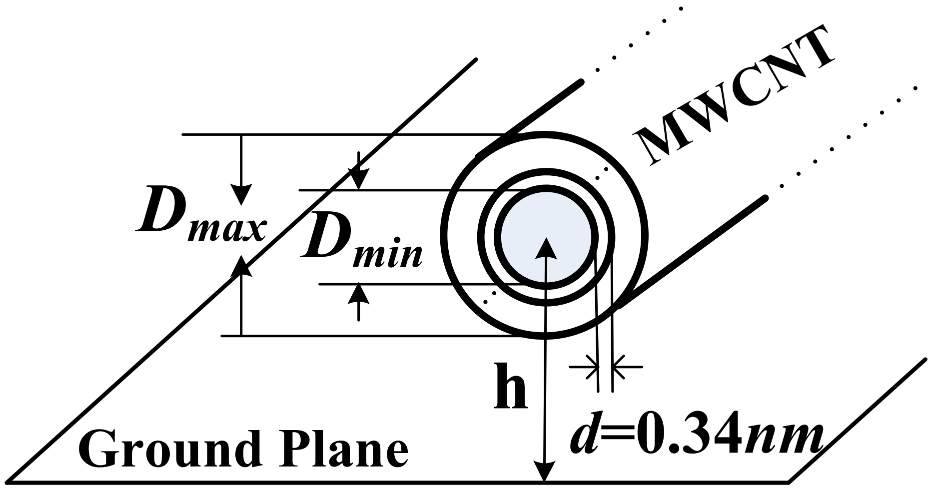
Equivalent circuit model of a tri-SWCNT bundle interconnect.

Tri-DWCNT Bundle TL

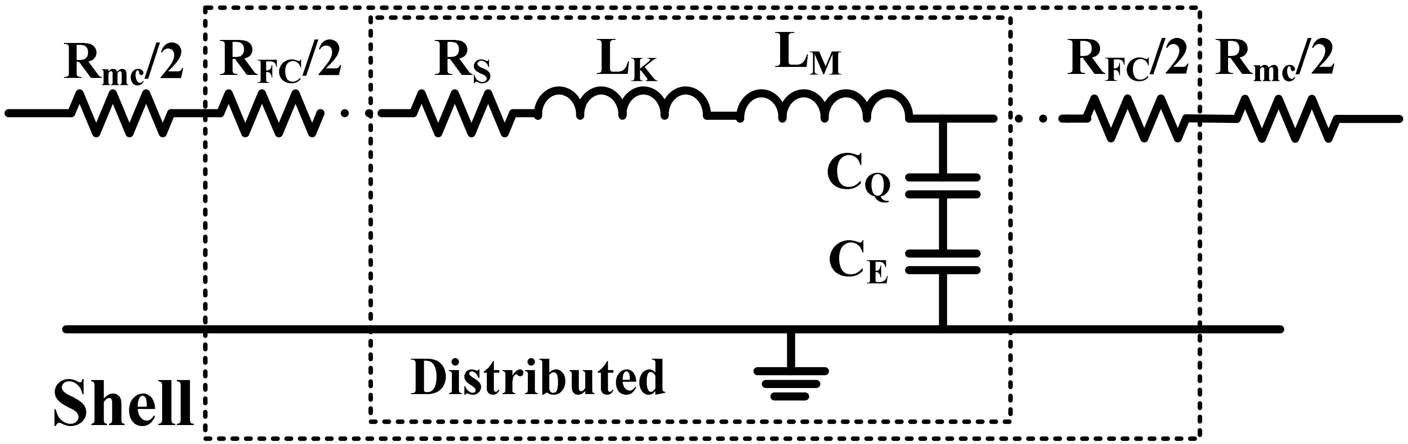


Equivalent circuit model of a tri-DWCNT bundle interconnect.

MWCNT TL

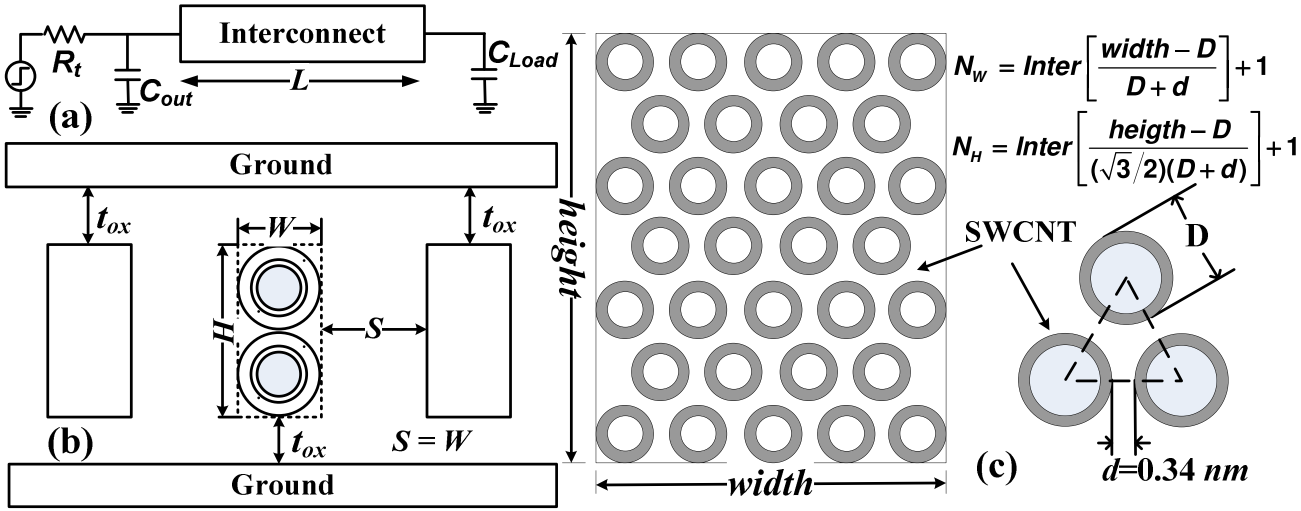


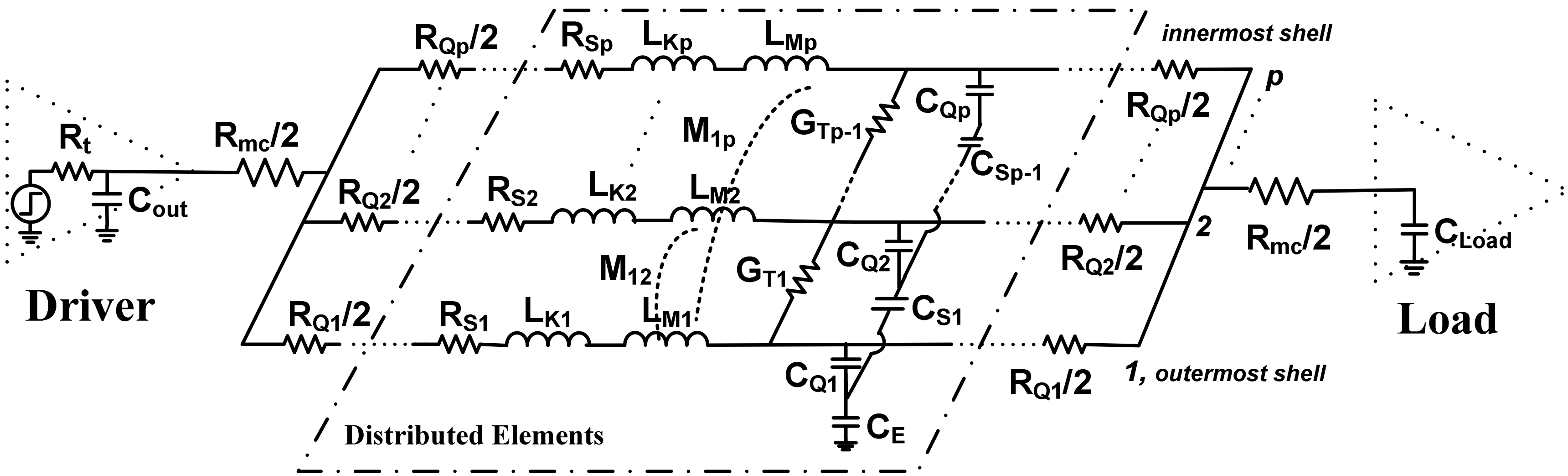
MWCNT
D_{max}
D_{min}
h
d=0.34nm
Ground Plane



$R_{mc}/2$
$R_{FC}/2$
R_S
L_K
L_M
C_Q
C_E
$R_{FC}/2$
$R_{mc}/2$
Shell
Distributed

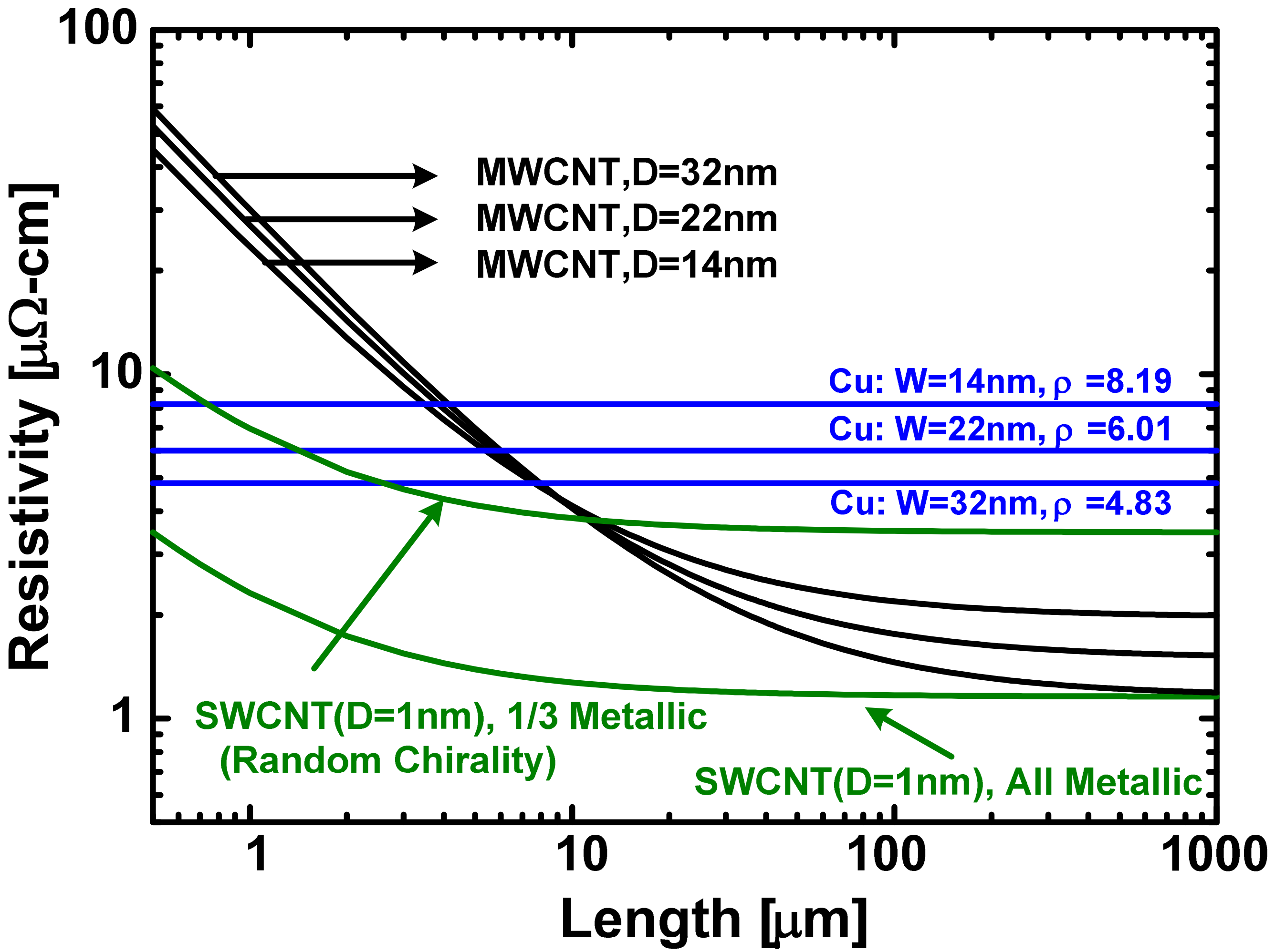
MWCNT Bundle TL





•H. Li, W. Y. Yin, J. F. Mao, and K. Banerjee, "Circuit modeling and performance analysis of multi-walled carbn nanotube(MWCNT)
•interconnects," *IEEE Trans. Electron Devices,* 55(6), 1328-1337, 2008.

Resistivity Comparison



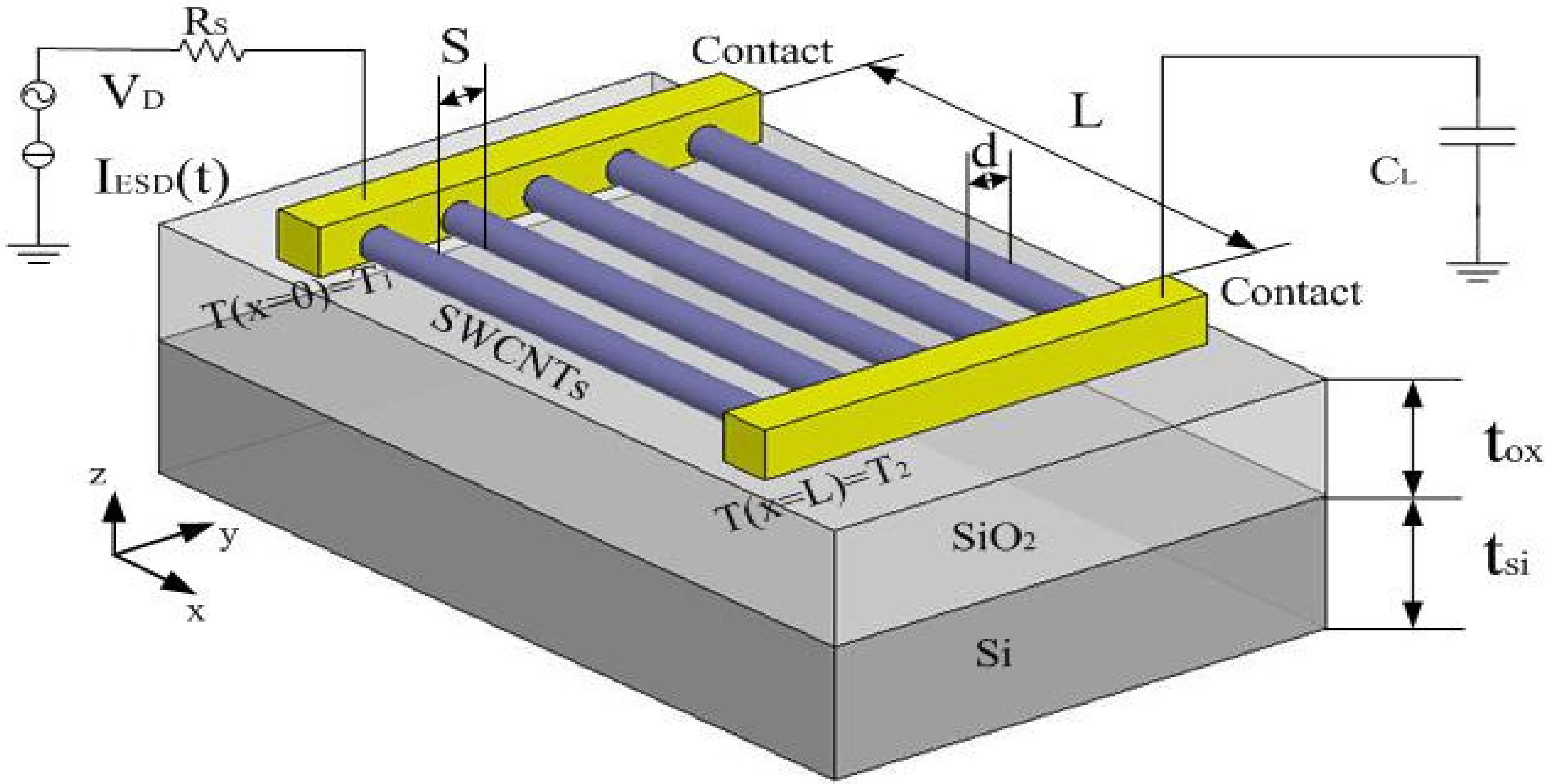
Comparison of resistivity among MWCNTs with various diameters, Cu wires with different dimensions, and SWNCT bundles with different chiralities. Dimension of Cu wires are adopted from ITRS. SWCNT bundles are assumed to be densely packed.

Problems

(1) How to get the breakdown voltage of a SWCNT?

(2) How to get the peak power handling capability of a SWCNT?

SWCNT ARRAY



Rs
VD
IESD(t)
S
Contact
L
d
CL
Contact
T(x=0)=T1
SWCNTs
T(x=L)=T2
tox
tsi
SiO2
Si
z
y
x

1-D Heat Conducting Equation

$$\begin{cases} \rho(T)c(T)\dfrac{dT(V,L,t)}{dt} = A\dfrac{d}{dx}[\kappa(T,L)\dfrac{d}{dx}T(V,L,t)] + p' - g(T-T_0) \\ T(x=0) = T_1 \\ T(x=L) = T_2 \end{cases}$$

$$p'(V,T(x),L) = I^2(V,T,L)\frac{dR(V,T(x),L)}{dx}\frac{h}{4q^2}\frac{1}{\lambda_{eff}(V,T(x),L)}$$

$$R(V,T,L) = R_C + \frac{h}{4q^2}\left[1 + \int_{-L/2}^{L/2}\frac{dx}{\lambda_{eff}(V,T(x),L)}\right]$$

elastic electron scattering of acoustic phonon

inelastic electron scattering caused by optical phonon emission

$$\lambda_{eff}(V,T(x),L) = \left(\lambda_{AC}^{-1} + \lambda_{OP,ems}^{-1} + \lambda_{OP,abs}^{-1}\right)^{-1}$$

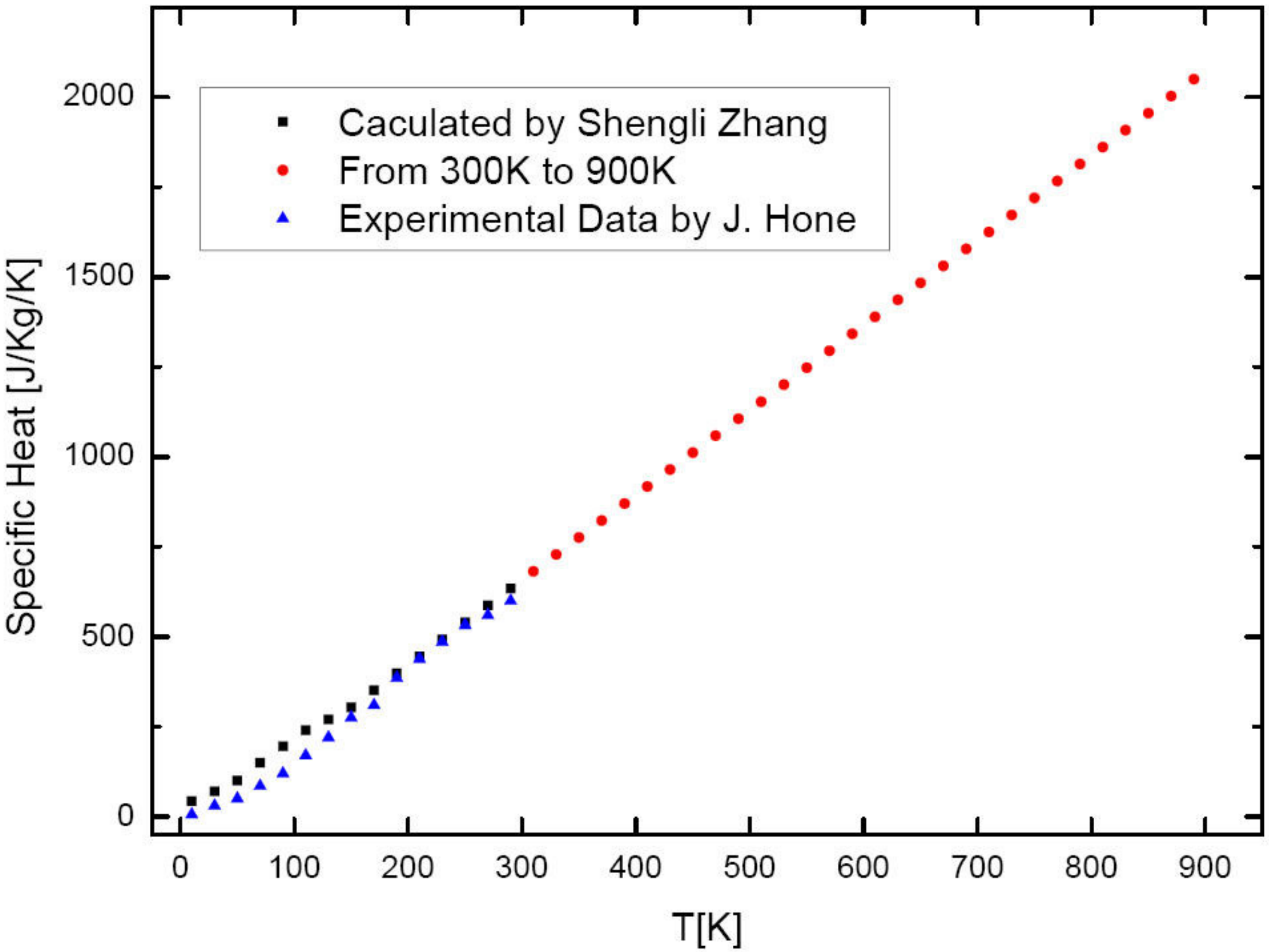
inelastic electron scattering caused by optical phonon absorption

$$\lambda_{AC} = \lambda_{AC,300}\left(\frac{300}{T}\right)$$

$$\lambda_{OP,ems} = \left(1/\lambda_{OP,ems}^{fld} + 1/\lambda_{OP,ems}^{abs}\right)^{-1}$$

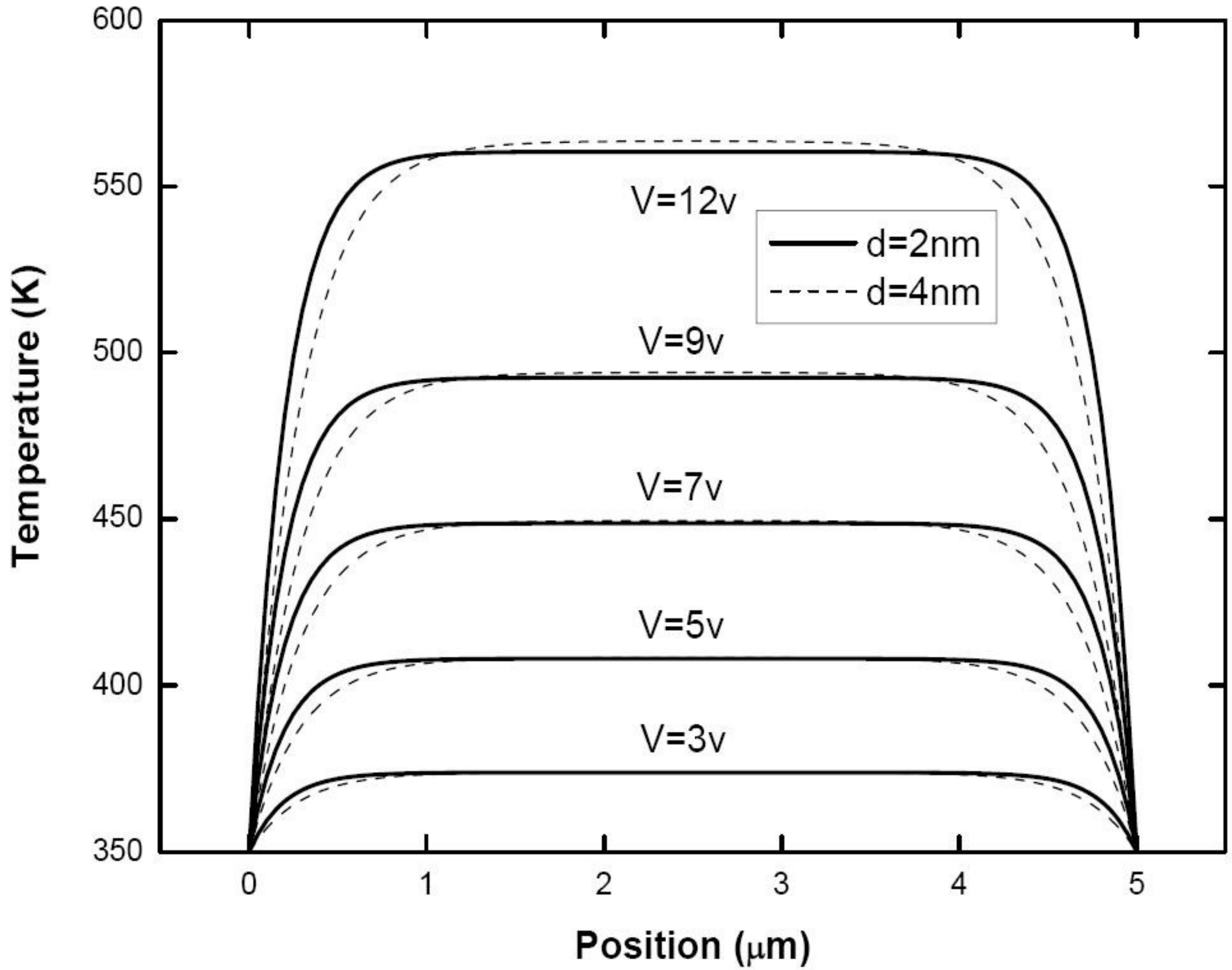
$$\kappa(T,L) = [3.7\times10^{-7}T + 9.7\times10^{-10}T^2 + 9.3(1+0.5/L)T^{-2}]^{-1}$$

Specific Heat



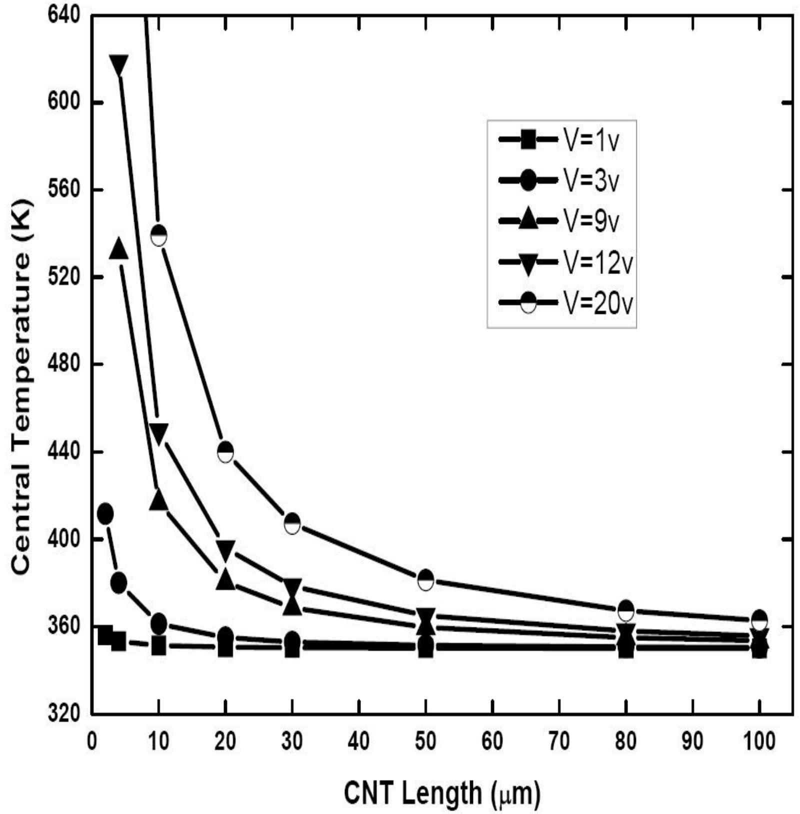
Specific heat of a SWCNT as a function of temperature

Temperature Distribution

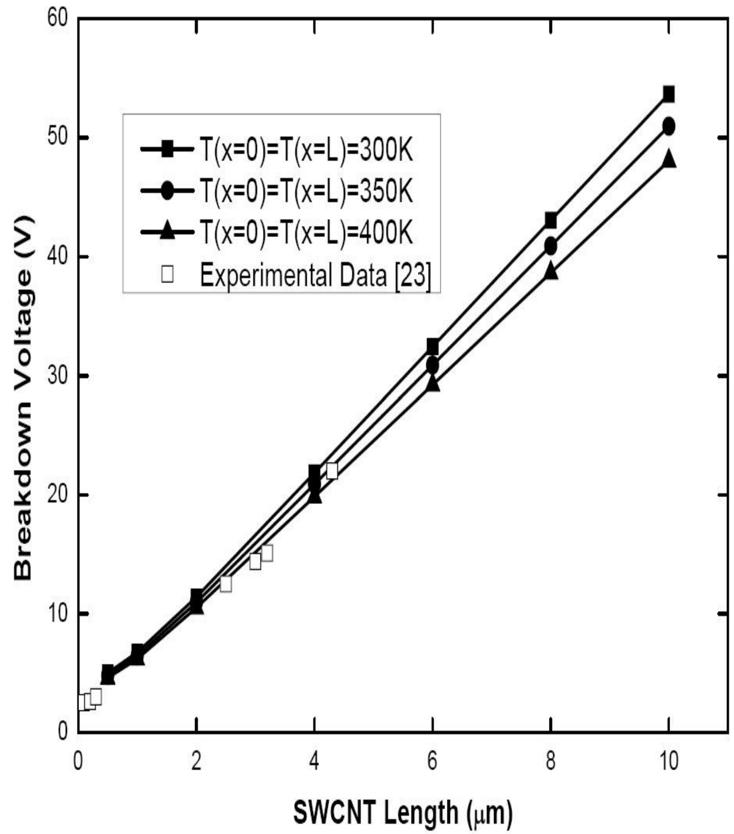


Longitudinal temperature distribution along single SWCNT in a SWCNT array biased by different voltages, respectively, where the total contact resistance is assumed to be 100Kohm.

Breakdown Voltage

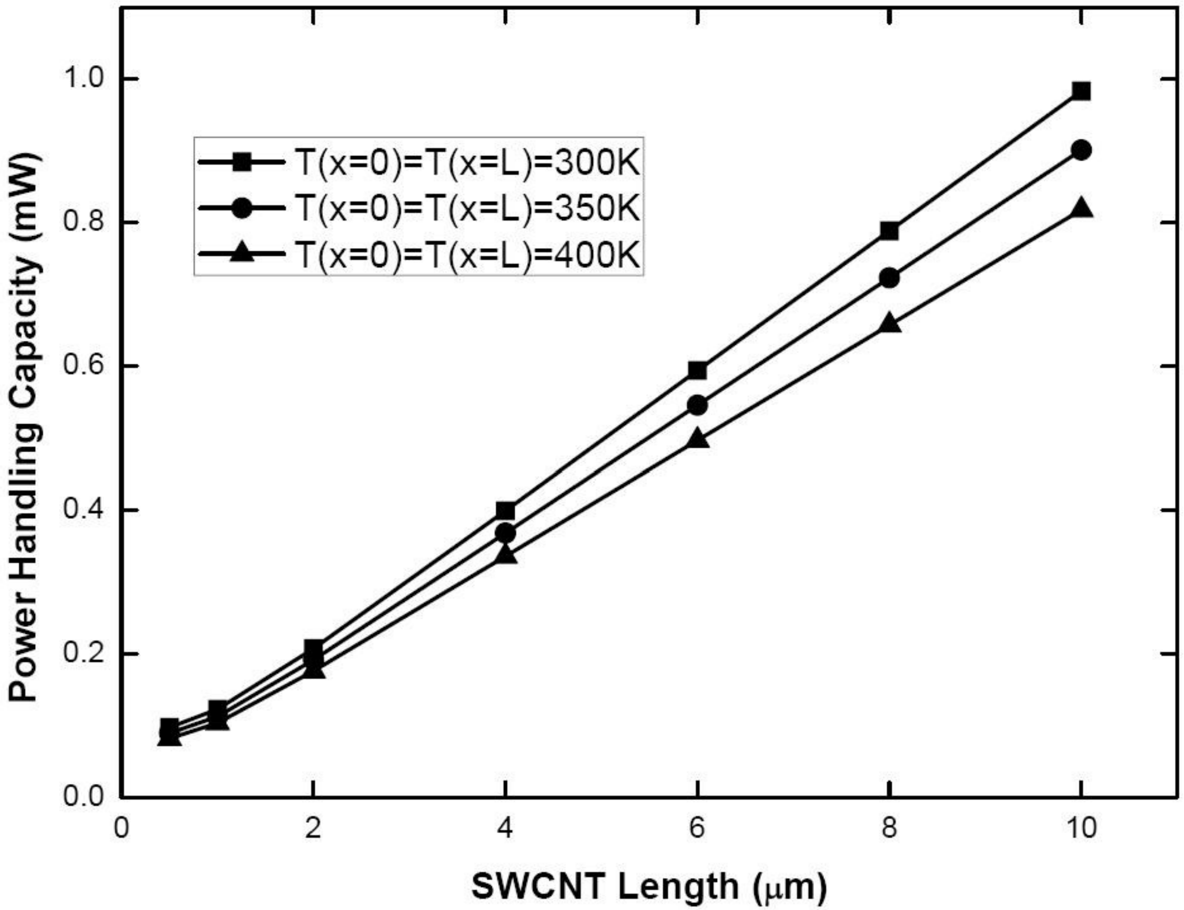


The highest central temperature of the SWCNTs in the array as a function of length biased by different voltage, respectively.



Breakdown voltage of the SWNCT local interconnect as a function of its length for different ambient temperatures at the input and output of the array, respectively.

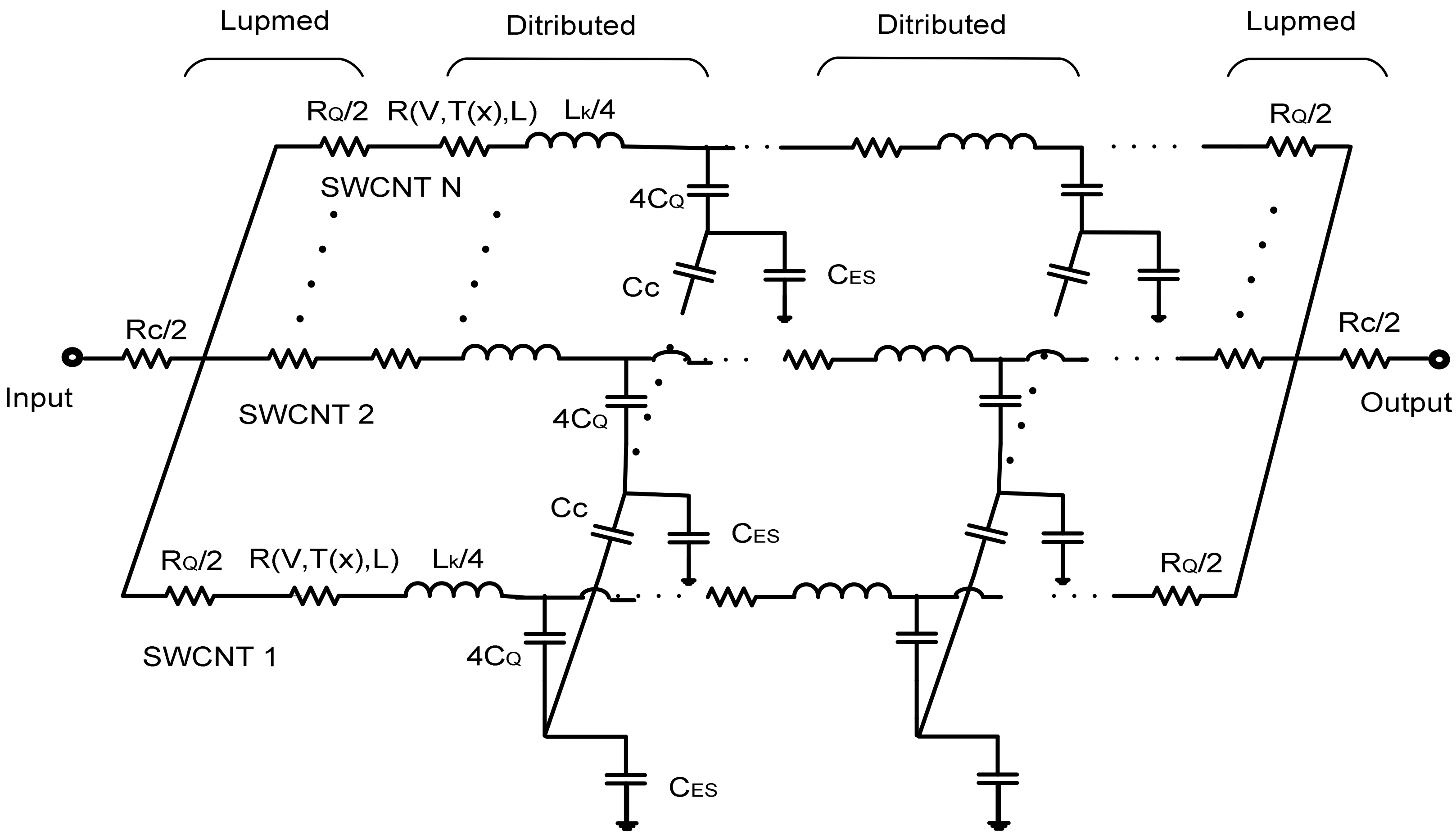
Power Handling Capability



Power handling capacity of the SWNCT local interconnect as a function of its length for different ambient temperatures at the input and output of the array, respectively.

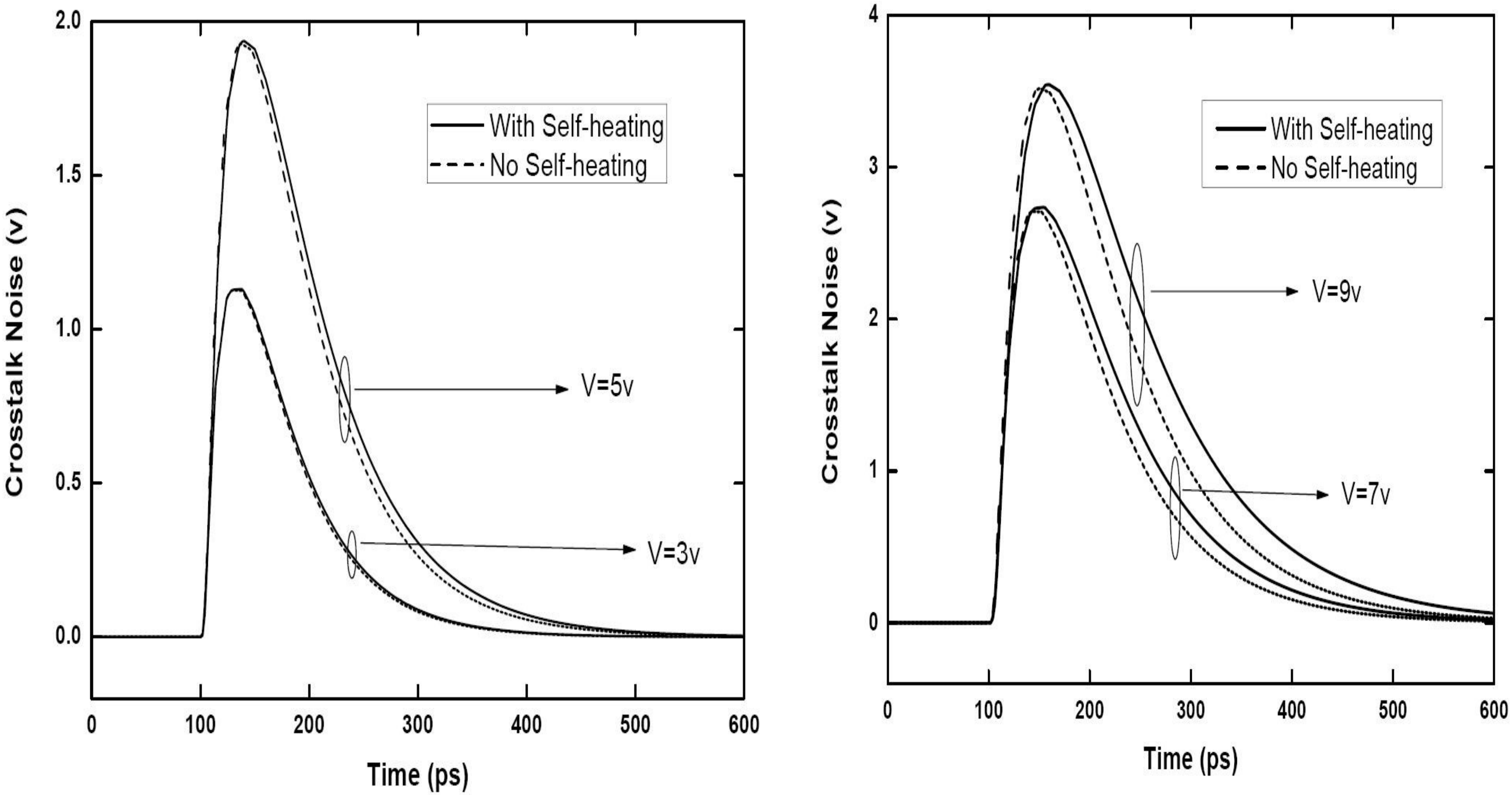
W. C. Chen, W. Y. Yin, *et al.*, "Electrothermal characterization of single-walled carbon nanotube (SWCNT) interconnect arrays," *IEEE Trans. Nanotechnology*, 8(6), 718-728, 2009.

Electro-thermal Equivalent Circuit Model



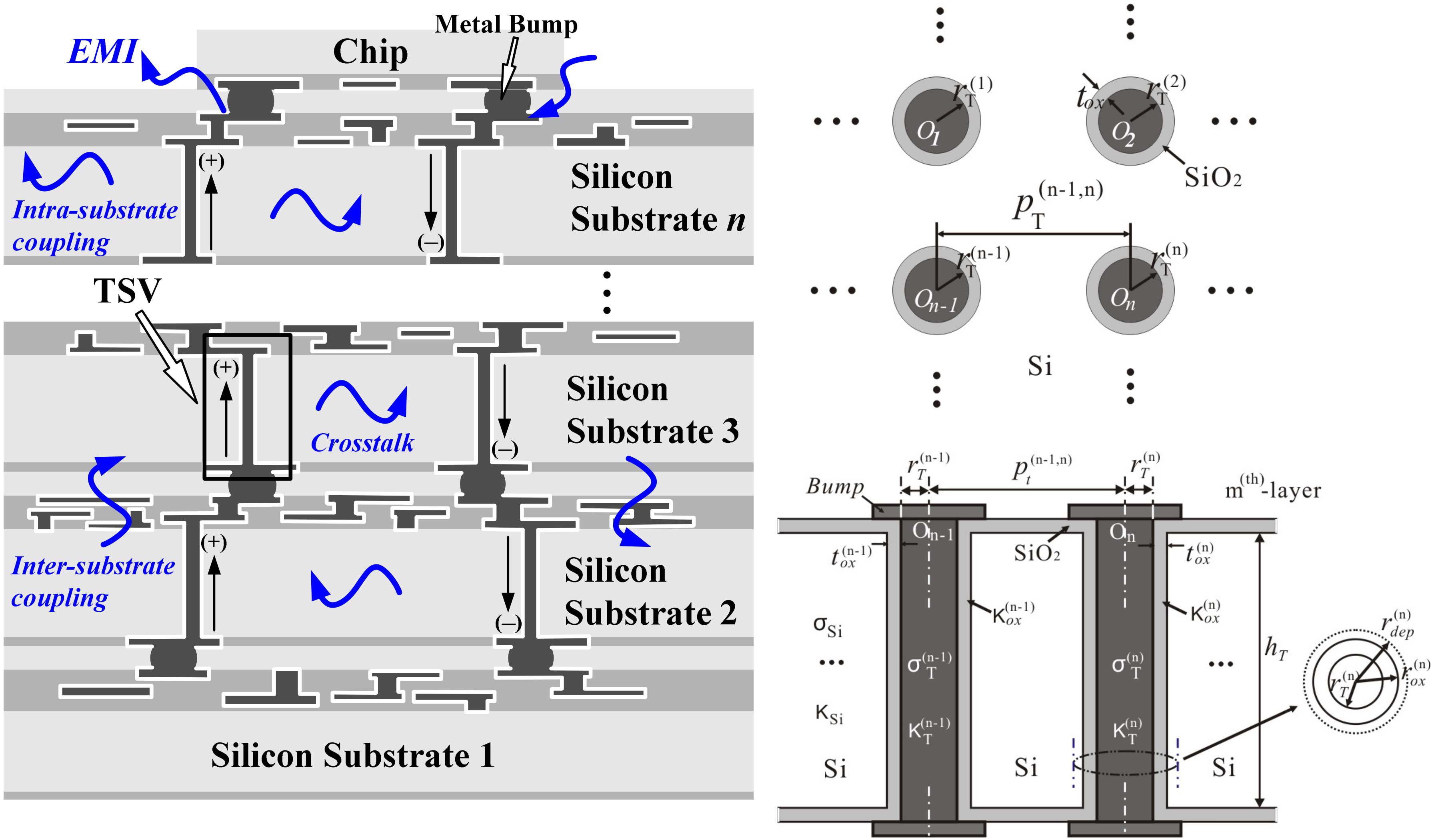
Electro-thermal equivalent circuit model of a metallic SWCNT N-array.

Self-heating Effect



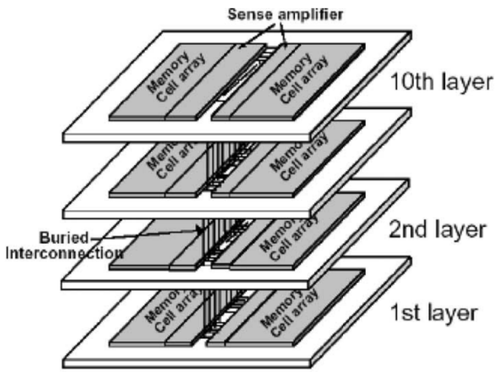
Crosstalk noise on the victim line in various biasing conditions with SWCNT length of 5 um.

Modeling of TS-MWCNTVB

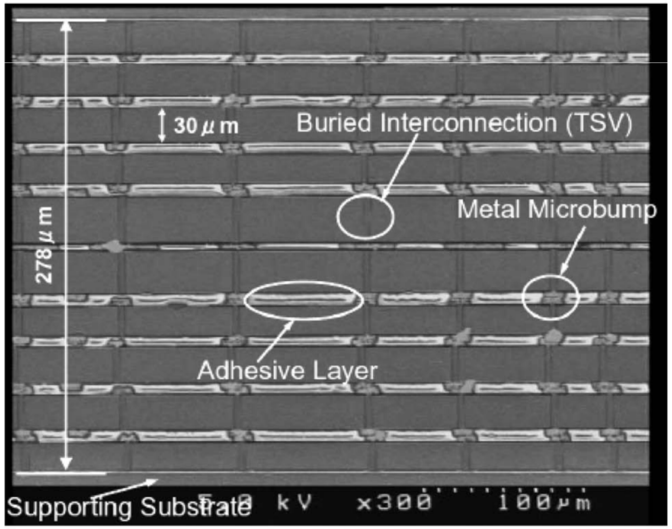


Key technology in 3-D ICs and advanced packaging systems

TSV: Key Technique for Real 3-D ICs

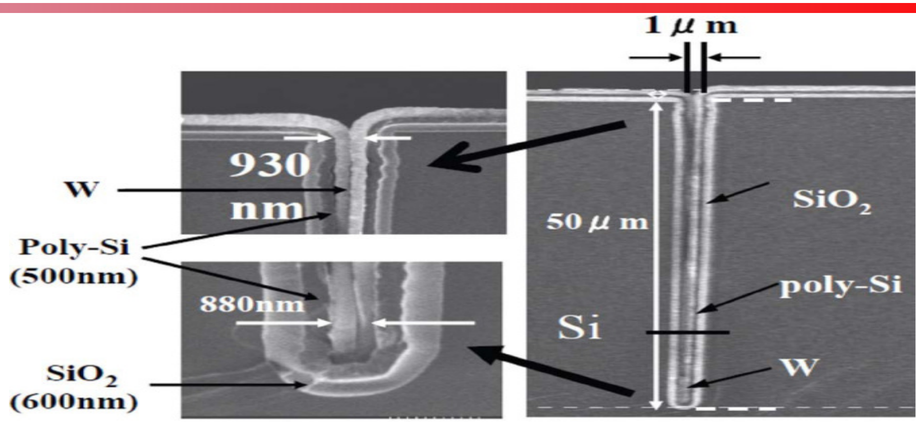


(a)

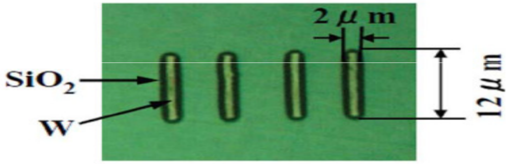


(b)

(a) Configuration of 3-D shared memory test chip
(b) an SEM cross-sectional view of it.

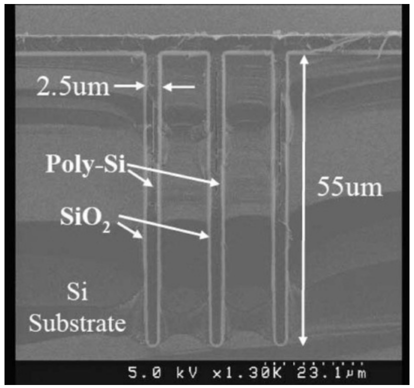


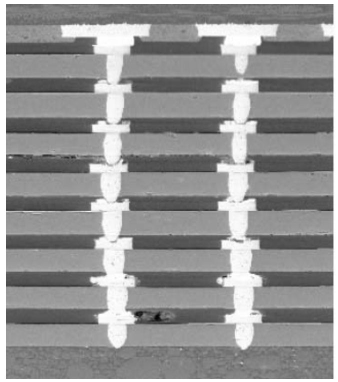
(a)



(b)

Cross-sectional view of the W/poly-Si TSV



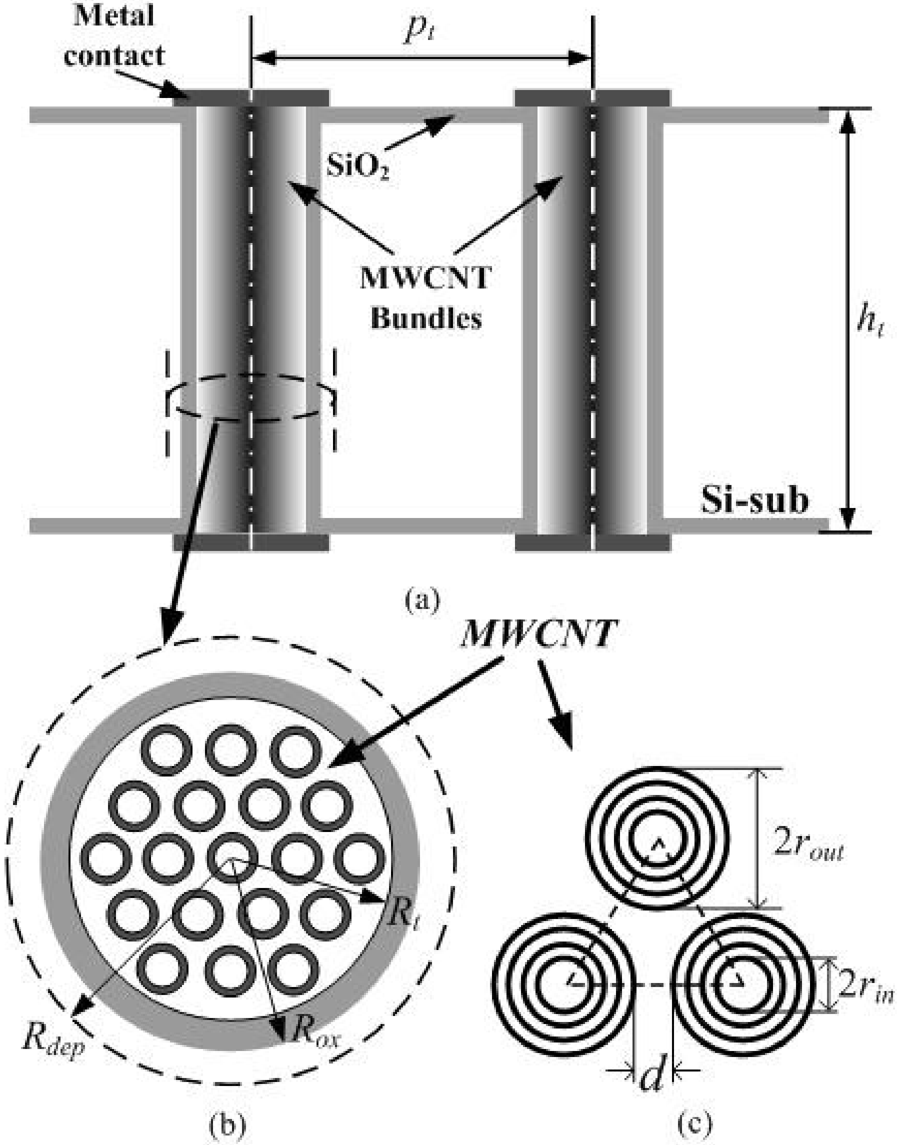


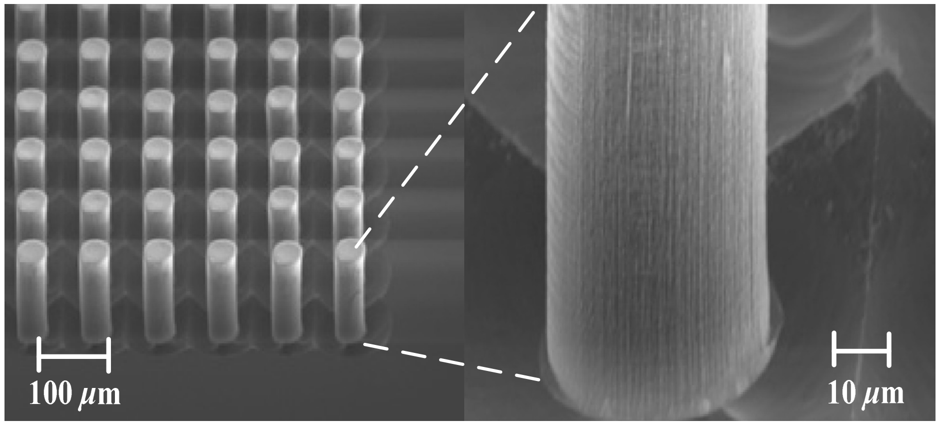
M. Koyanagi, T. Fukushima, and T. Tanaka, “High-density through silicon vias for 3-D LSIs,” *Proc. IEEE*, vol.97, no.1, pp.49-59, 2009.

Problem

(1) Main advantages of using through silicon vias for 3-D ICs and Packaging?

Modeling of TS-MWCNTBV





T. Wang, K. Jeppson, *et al.*, *Nanotechnol.*, 20(48), 2009.

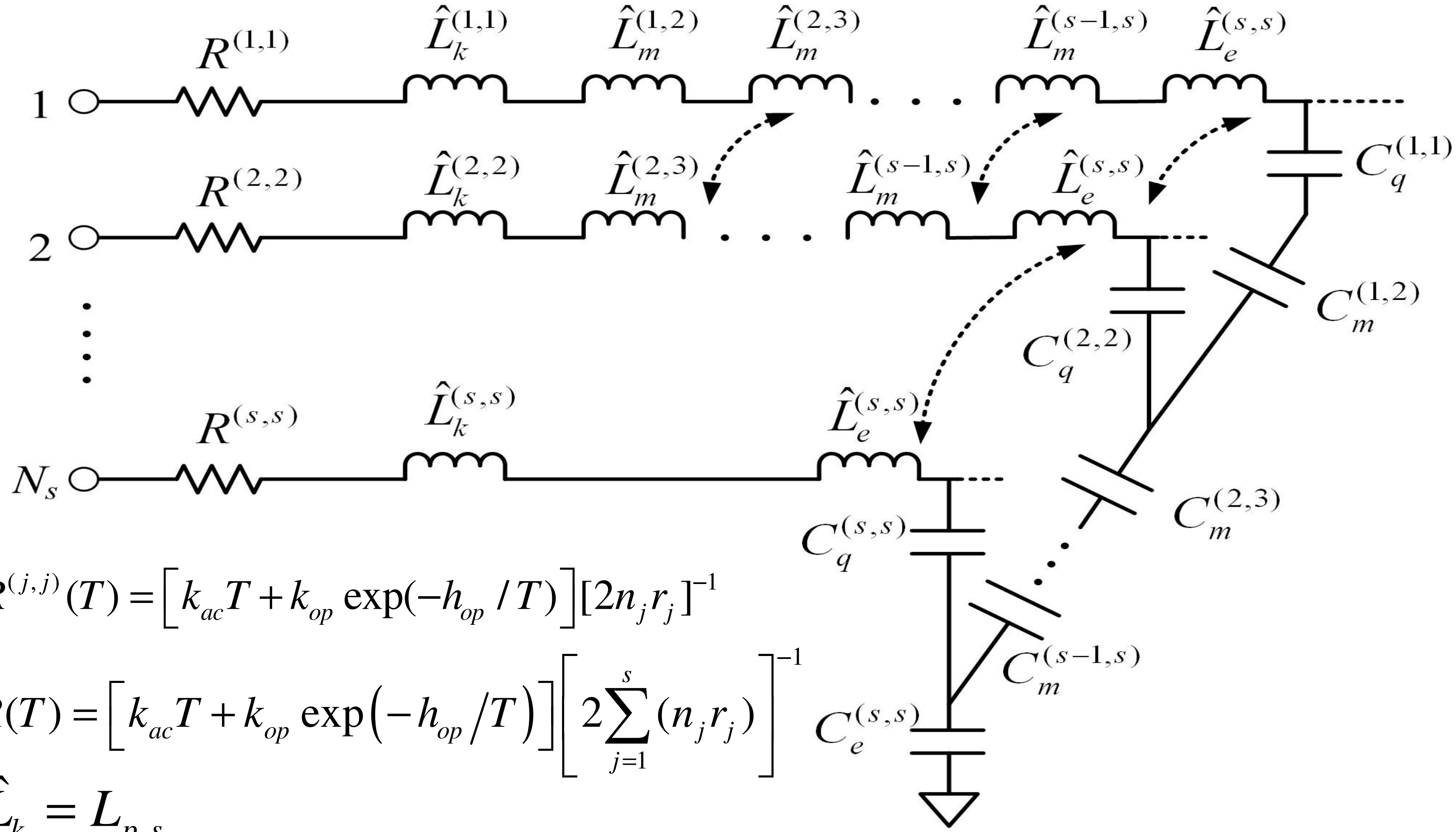
J. P. Cui, W.S. Zhao, and Wen-Yan Yin, *IEEE Trans. Electron Devices*, 2011 (revised for publ.)

Problems

(1) The difficulties of using single CNT or MWCNT to built a via?

(2) Temperature effects on thermal conductivities of SWCNT and MWCNT bundles?

Circuit Model of Single MWCNT



$$R^{(j,j)}(T) = \left[k_{ac}T + k_{op}\exp(-h_{op}/T)\right][2n_j r_j]^{-1}$$

$$\hat{R}(T) = \left[k_{ac}T + k_{op}\exp\left(-h_{op}/T\right)\right]\left[2\sum_{j=1}^{s}(n_j r_j)\right]^{-1}$$

$$\hat{L}_k = L_{p,s}$$

$$\hat{C}_q = C_{p,s}$$

$$Z_{CNT,self}^{(j,j)}(T) = (R_{mc}^{(j,j)} + R_Q^{(j,j)} + R^{(j,j)}(T) + j\omega\hat{L}_k^{(j,j)})/n_j$$

M. D'Amore, M. S. Sarto, and A. Tambrrrano, *IEEE Trans. Electromagn. Compat.*, 52(2), 2010.

Modeling of A Couple of TS-MWCNTBVS

dopant impurity concentration:

$$\mu_p(300\text{ K}) = \frac{\mu_{\max} - \mu_{\min}}{1 + (N_a / N_{ref})^{\alpha}} + \mu_{\min}$$

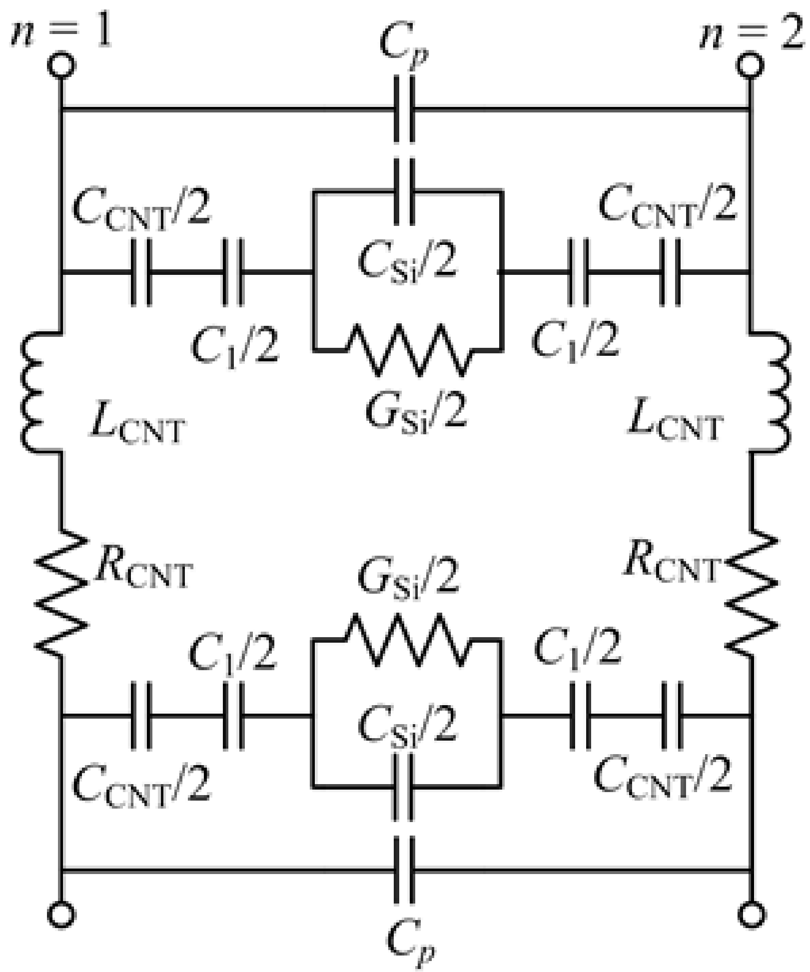
$$\sigma_{\text{Si}}(T) = 1.602 \times 10^{-17} N_a \mu_p(T)$$

$$R_{CNT} = R_{inner} + R_{sub}/2$$

$$C_{CNT} = \hat{C}_q \cdot N_{CNT}$$

$$C_{\text{Si}} = \pi\varepsilon_{\text{Si}} / \cosh^{-1}[0.5 p_t /(R_{dep})]$$

$$G_{\text{Si}} = \sigma_{\text{Si}} C_{\text{Si}} / \varepsilon_{\text{Si}}$$



$$L_{CNT} = L_{inner} + \frac{\mu}{2\pi}\ln\left(R_{dep}/R_t\right) + \frac{\mu}{4}\text{Im}\left[H_0^{(2)}\left((1-j)R_{dep}/\delta_{\text{Si}}\right)\right]$$

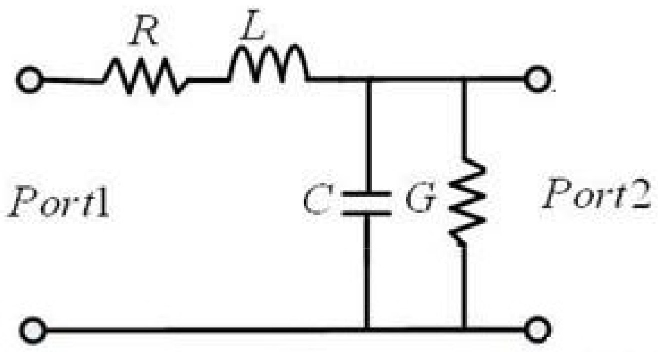
Most elements are both frequency- and temperature-dependent!

Modeling of A Couple of TS-MWCNTBVS

$$Y = \left[2\left(j\omega C_T \right)^{-1} + Y_1^{-1} \right]^{-1} = G + j\omega C$$

$$\sigma_{eff}(T) = h_t \cdot \frac{2}{\sqrt{3}} (2r_{out} + d)^{-2} \cdot \sum_{j=1}^{s} (Z_{CNT,self}^{(j,j)}(T))^{-1}$$

$$Y_1 = G_{\mathrm{Si}} + j\omega C_{\mathrm{Si}}$$



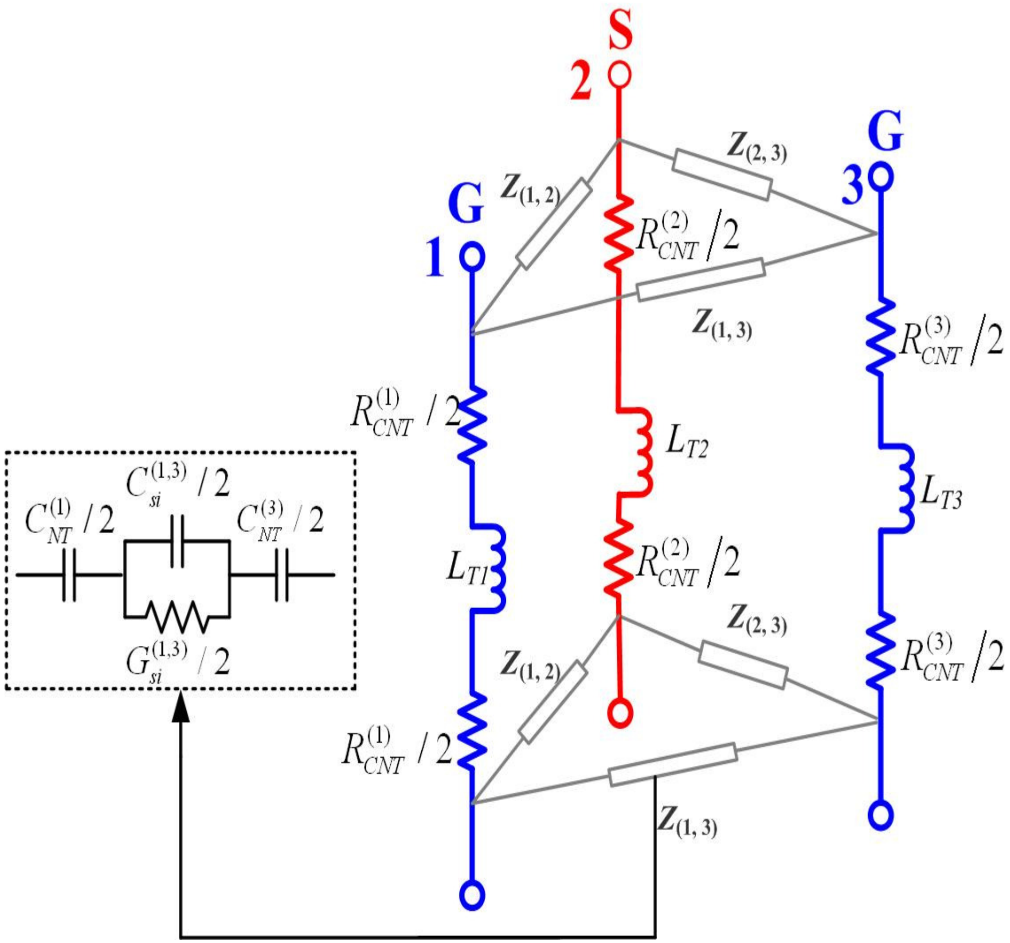
$$G = \left[\omega^2 G_{\mathrm{Si}} C_T^2 \ / \left(G_{\mathrm{Si}}^2 + \omega^2 \left(C_T + C_{\mathrm{Si}} \right)^2 \right) \right]$$

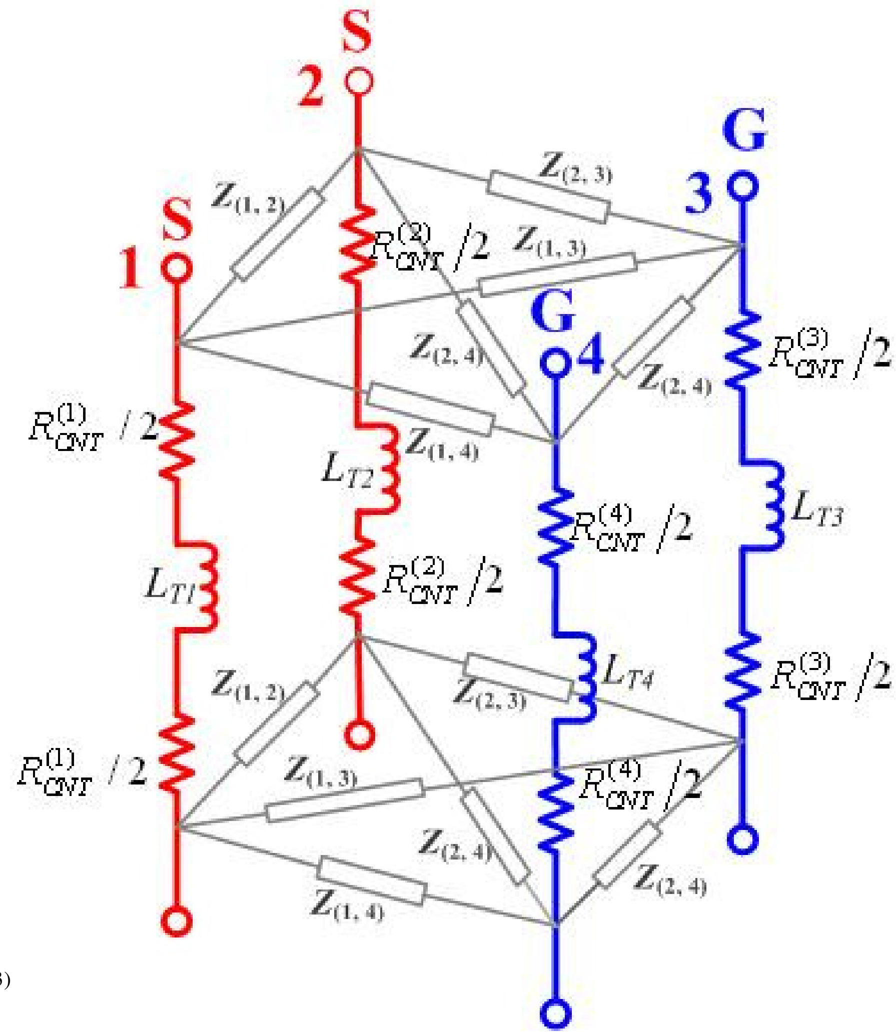
$$C = \left[\left(G_{\mathrm{Si}}^2 C_T + \omega^2 C_T C_{\mathrm{Si}} \left(C_T + C_{\mathrm{Si}} \right) \right) / \left(G_{\mathrm{Si}}^2 + \omega^2 \left(C_T + C_{\mathrm{Si}} \right)^2 \right) \right]$$

$$C_T = (C_{CNT}^{-1} + C_1^{-1})^{-1} / 2$$

Most elements are both frequency- and temperature-dependent!

Modeling of TS-MWCNTBV

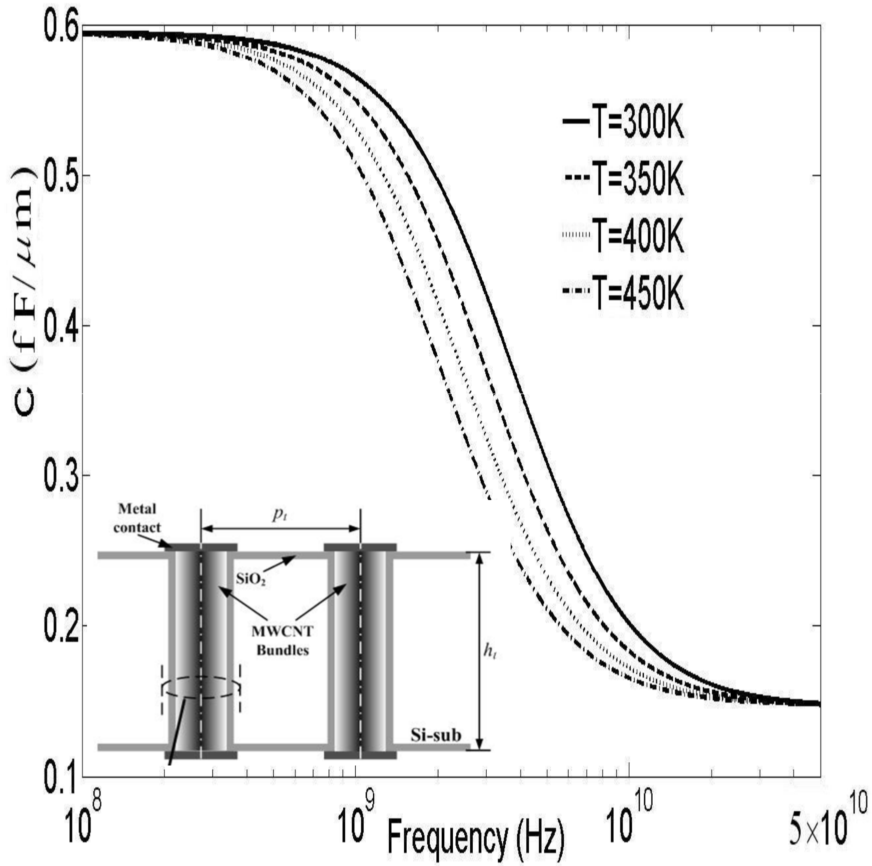


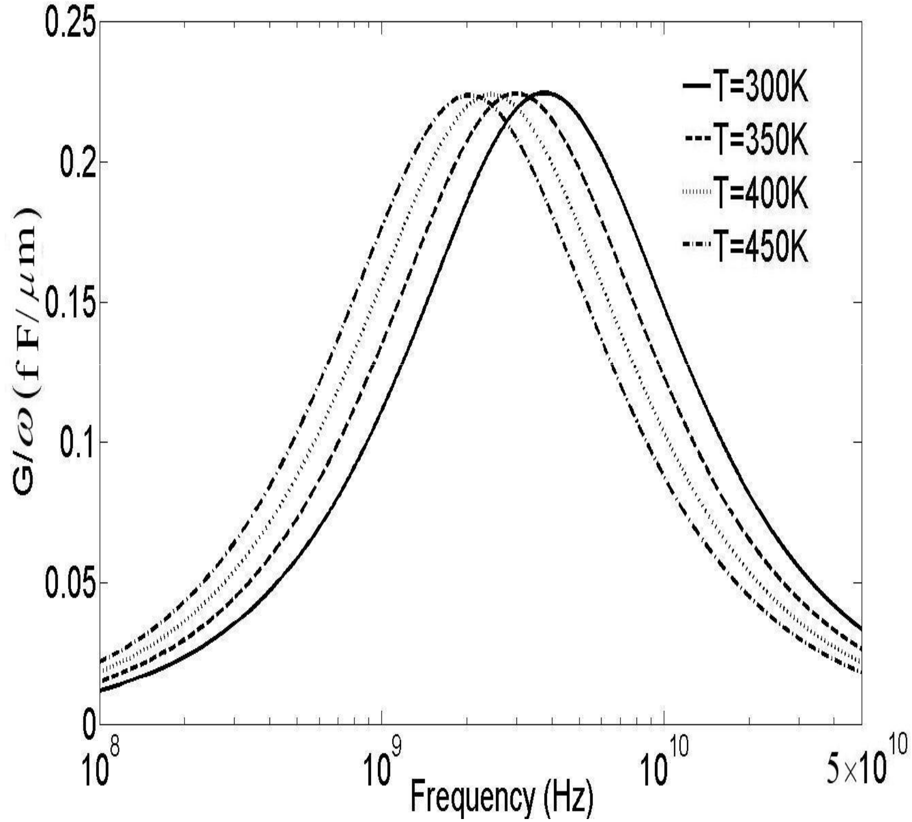


$$L_T^{(i)}|_{i=1,3} = L_{CNT}^{(i)} - M^{(i,2)} + M^{(1,3)}$$
$$= L_{CNT}^{(i)} - \frac{\mu}{4}\cdot \mathrm{Im}\left[H_0^{(2)}((1-j)p_t^{(i,2)}/\delta_{Si})\right]$$
$$+\frac{\mu}{4}\cdot \mathrm{Im}\left[H_0^{(2)}((1-j)p_t^{(1,3)}/\delta_{Si})\right]$$

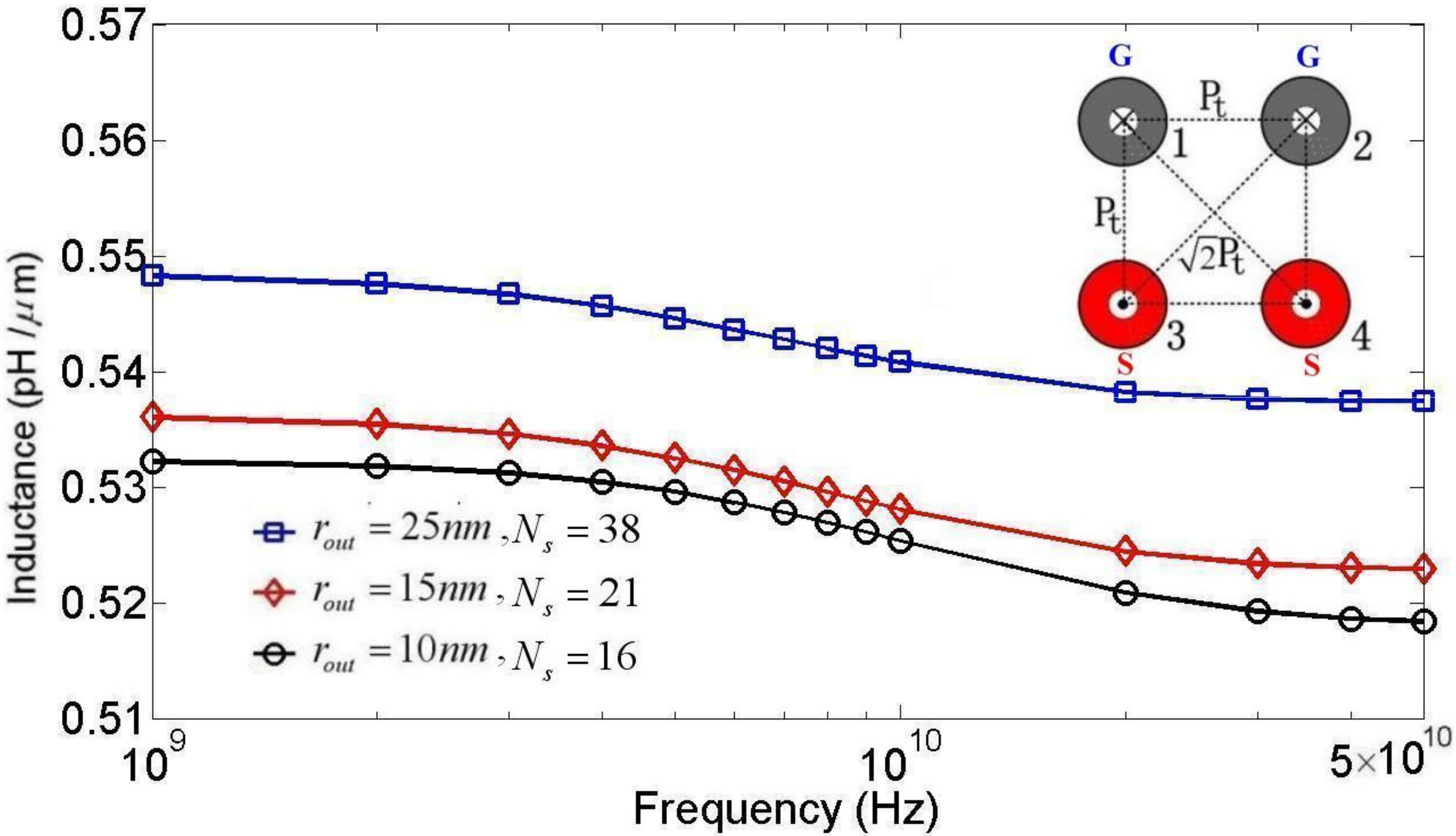
$$L_T^{(2)}| = L_{CNT}^{(2)} - M^{(1,2)} - M^{(2,3)}$$
$$= L_{CNT}^{(2)} - \frac{\mu}{4}\cdot \mathrm{Im}\left[H_0^{(2)}((1-j)p_t^{(1,2)}/\delta_{Si})\right]$$
$$-\frac{\mu}{4}\cdot \mathrm{Im}\left[H_0^{(2)}((1-j)p_t^{(2,3)}/\delta_{Si})\right]$$

Modeling of A Couple of MWCNTBV



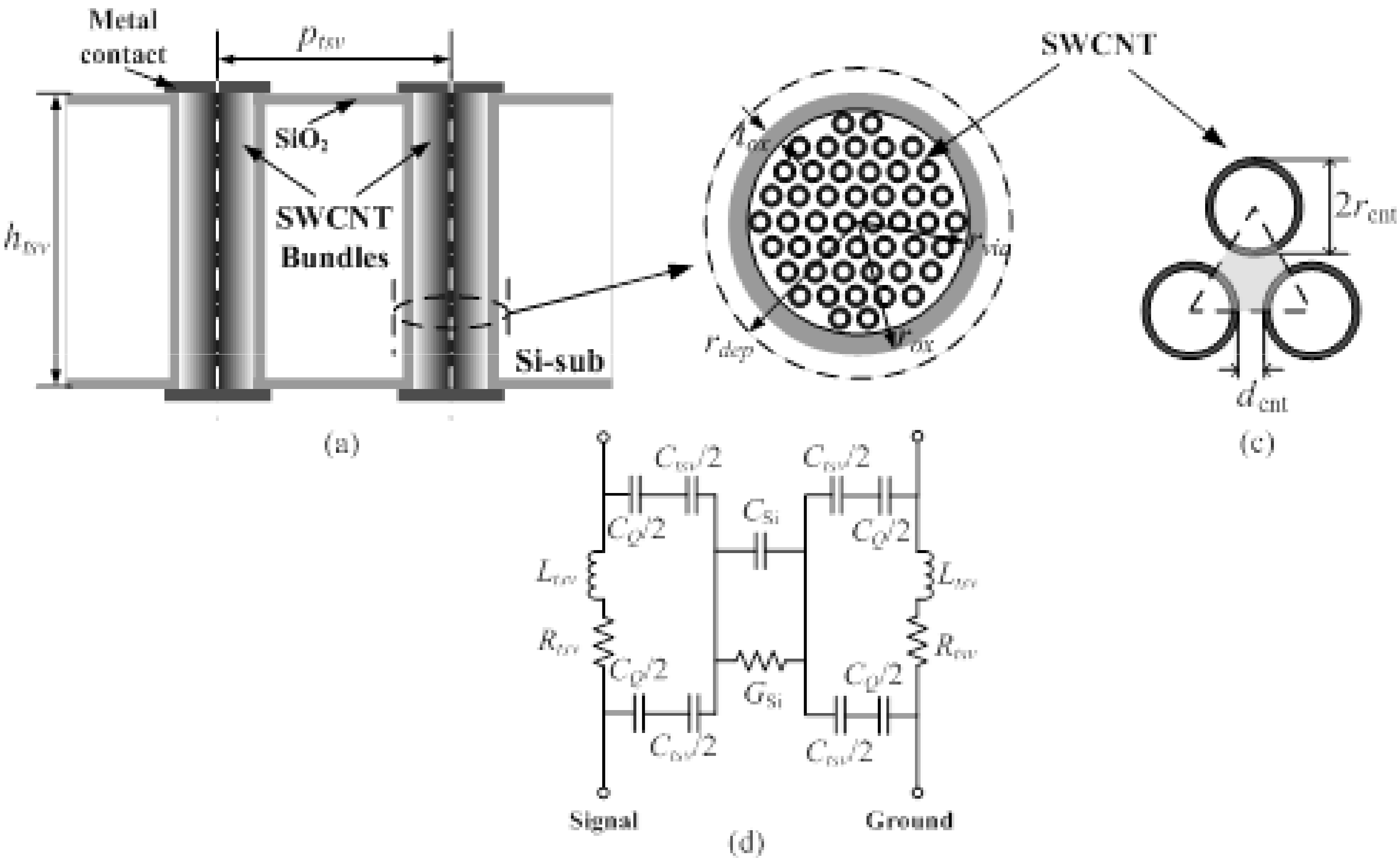


Modeling of 4 TS-MWCNTBV Array



Total inductance of each via in the 4-TS-MWCNTBV as a function of frequency for different outer radii

Modeling of A Couple of TS-SWCNTBV

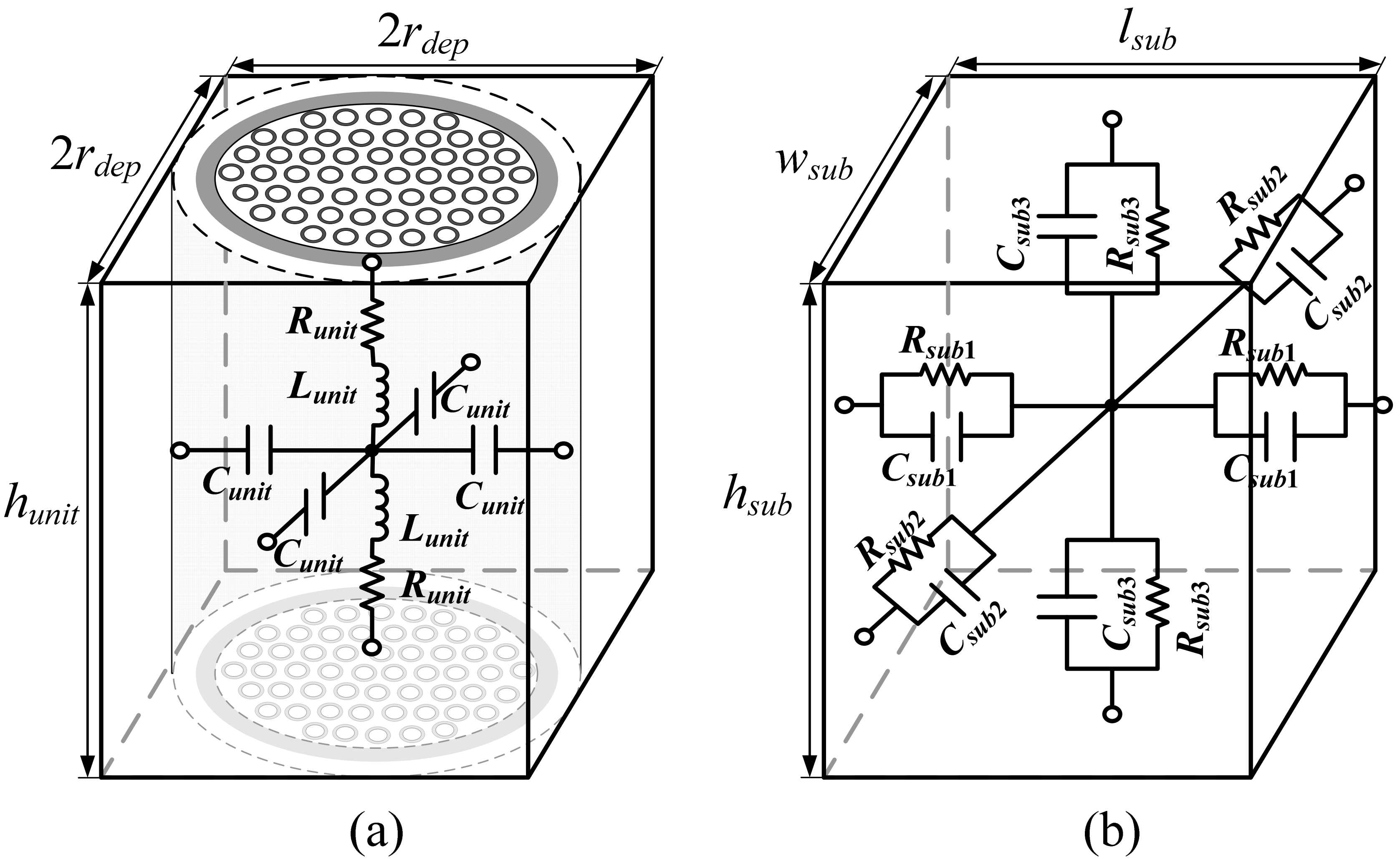


Problems

(1) The difficulties of charactering effective thermal conductivity of MWCNTB?

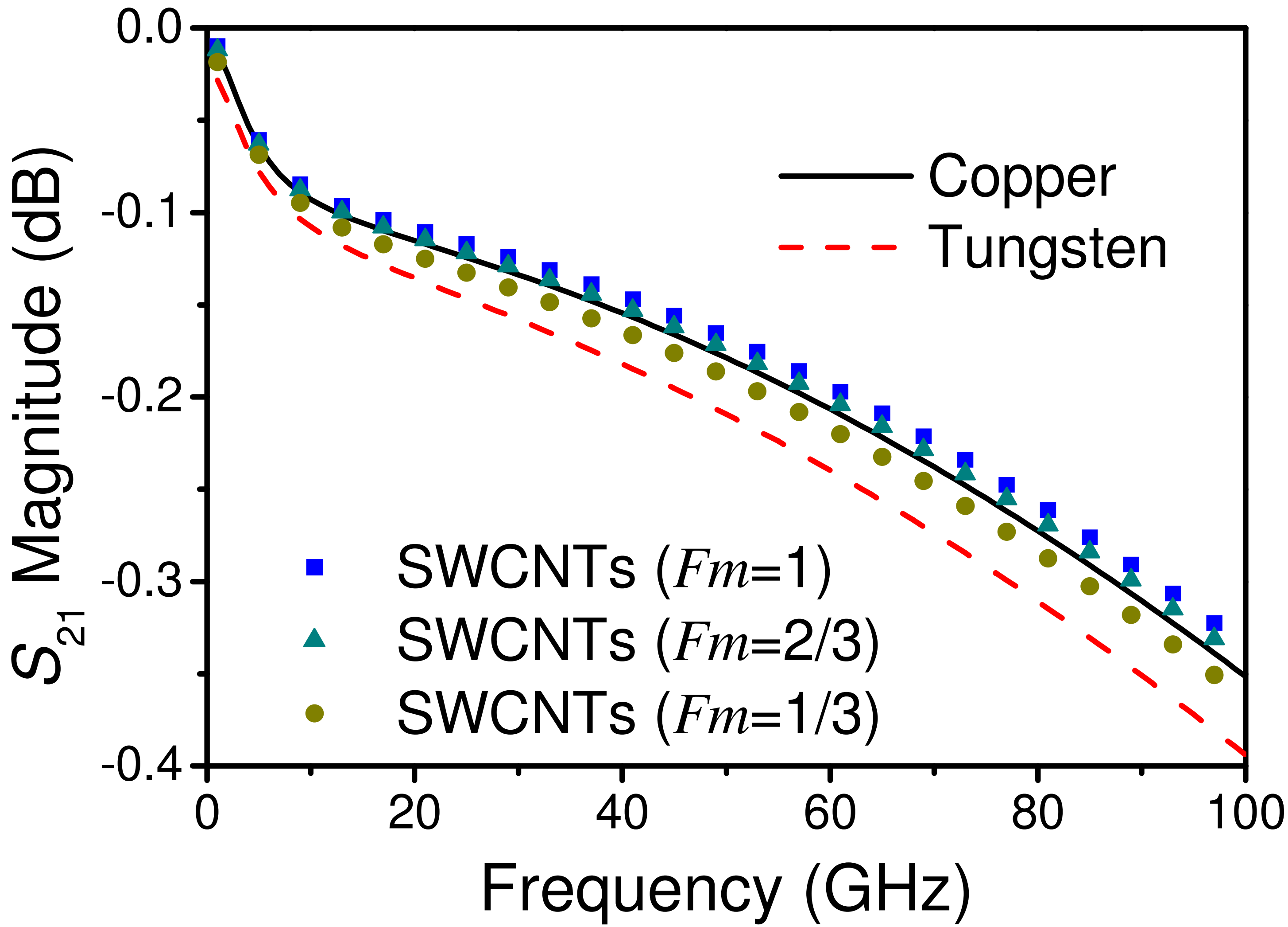
(2) The effective electrical conductivity of MWCNTB?

Modeling of TS-SWCNTBV



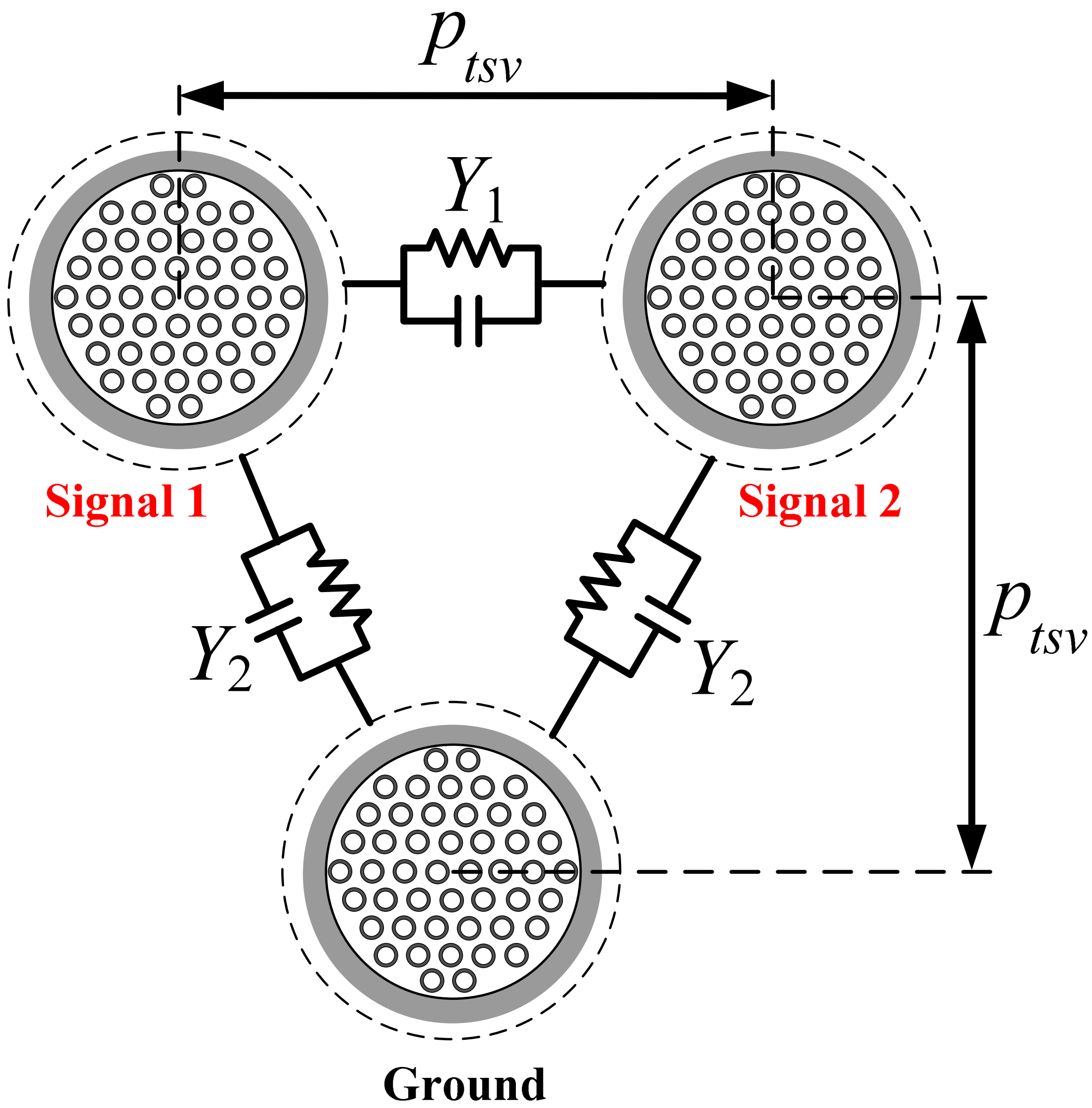
Equivalent circuit models of (a) TS-SWCNTBV unit cell, and (b) silicon substrate unit cell

Modeling of A Couple of TS-SWCNTBV

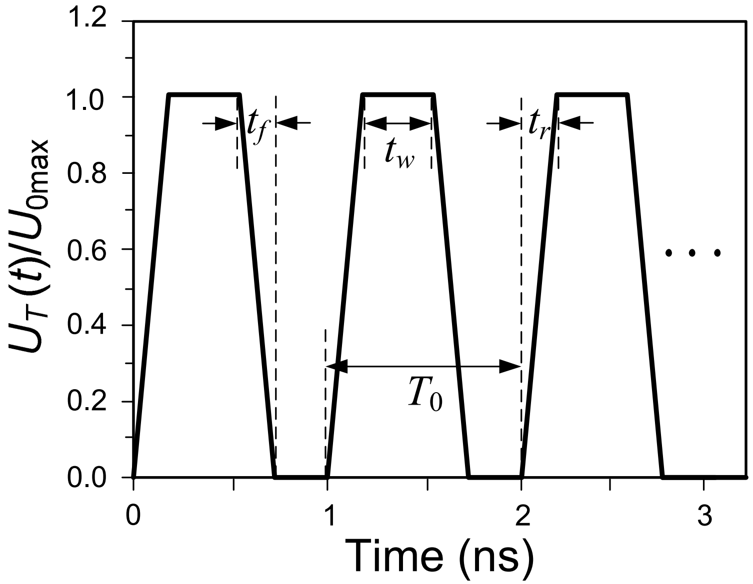


S-parameter for a pair of TSVs with the same geometry but made of SWCNTs, copper and tungsten, respectively. The radii of all SWCNTs are chosen to be 0.5nm.

Modeling of TS-SWCNTBV Array



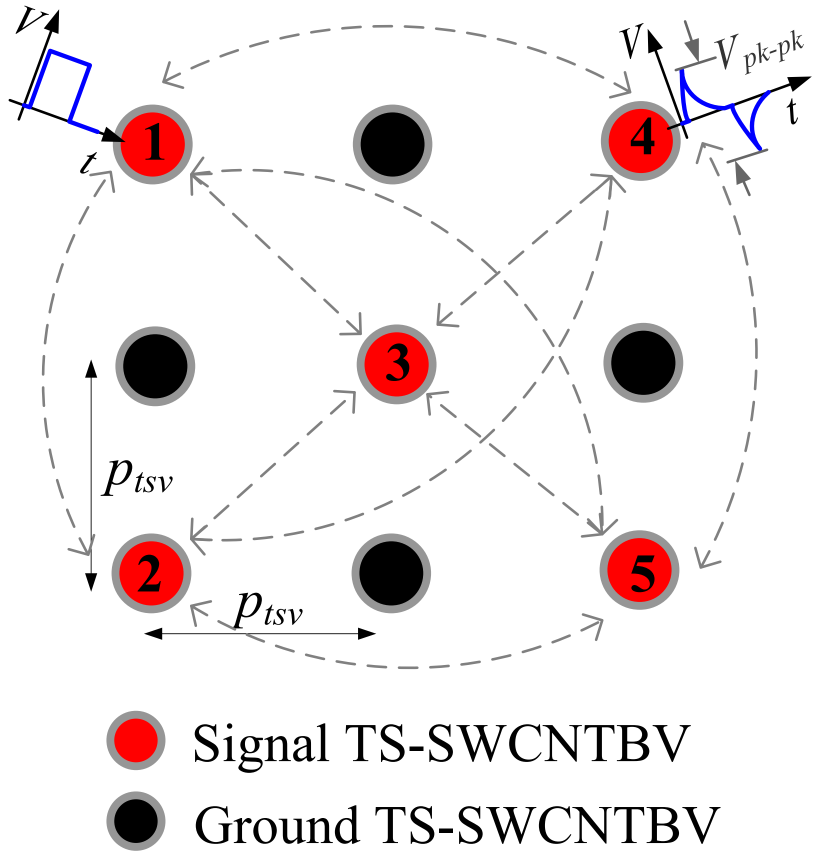
Coupling Noise in TS-SWCNTBV Array



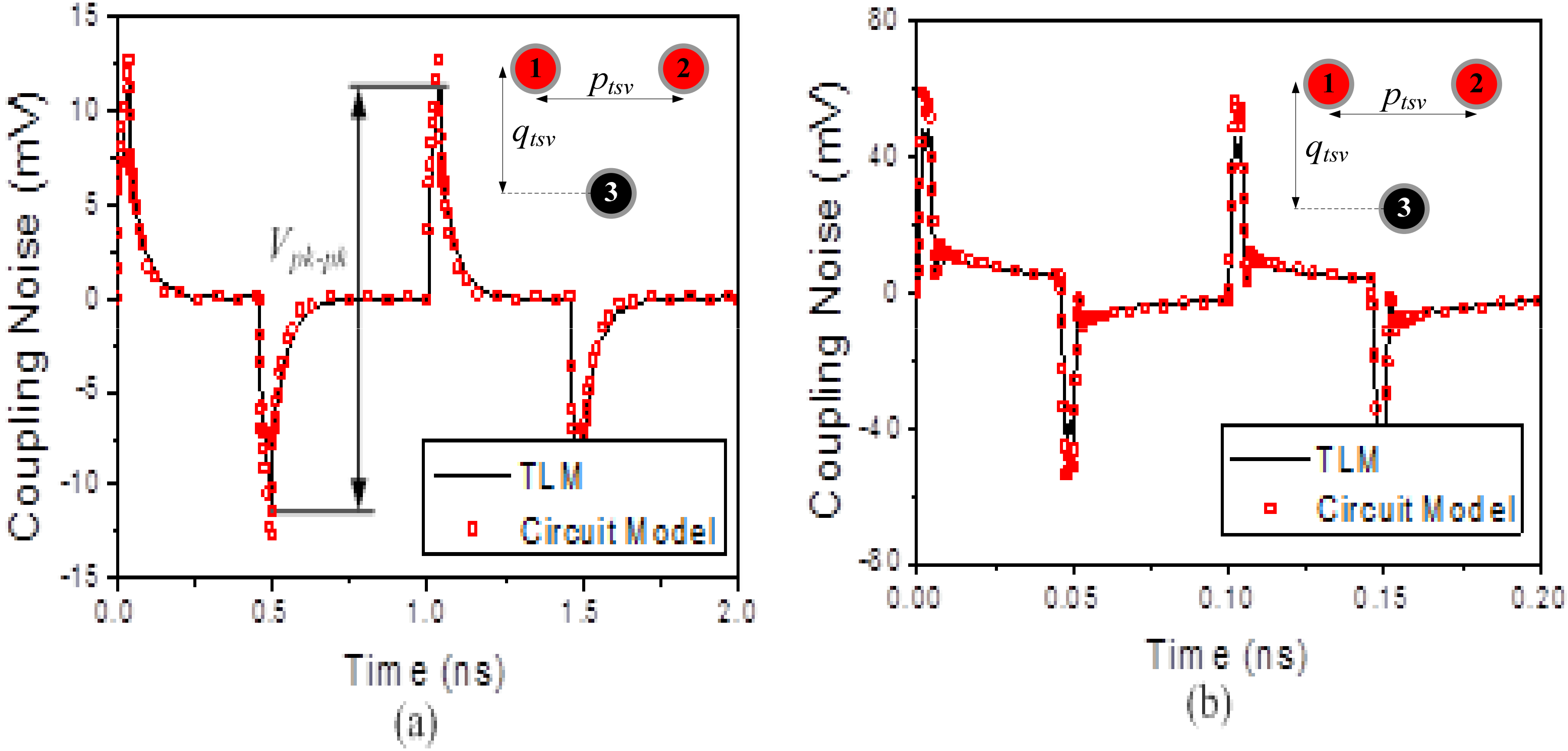
Waveform of the injected clock signal

$$U_T(t) = \sum_{i=0}^{n} U_0(t - iT_0)$$

$$U_0(t) = \begin{cases} U_{0\,\max} t/t_r, & t \le t_r \\ U_{0\,\max}, & t_r < t \le t_r + t_w \\ U_{0\,\max}[1 - (t - t_r + t_w)/t_f], & t_r + t_w < t \le t_r + t_w + t_f \\ 0, & t > t_r + t_w + t_f \end{cases}$$



Coupling Noise in TS-SWCNTBV Array

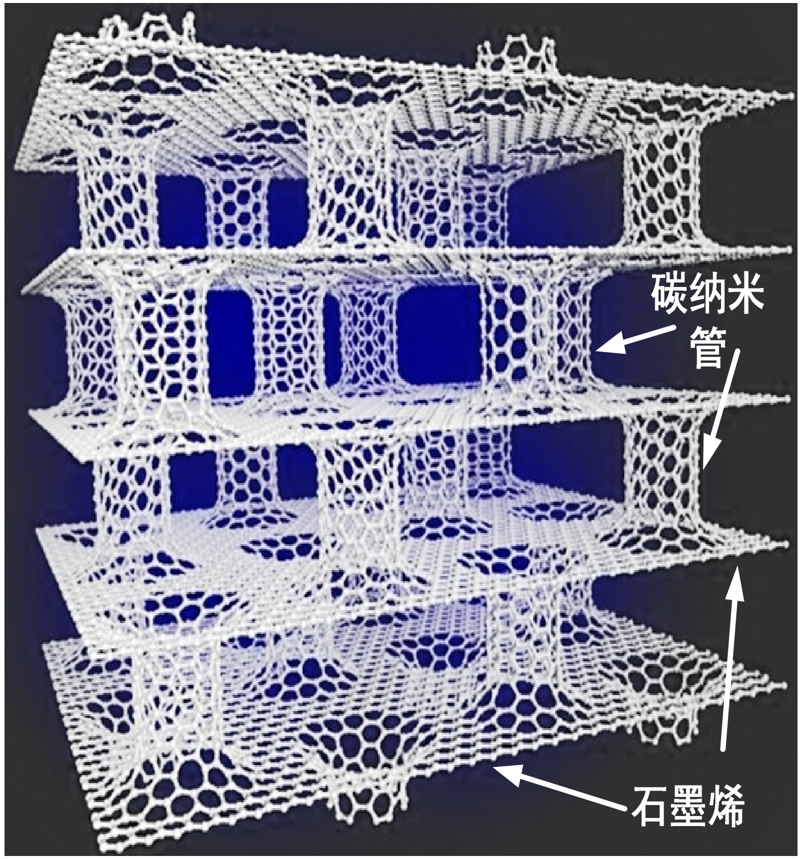


Coupling noise in 3-TS-SWCNTBV array obtained by TLM and the equivalent circuit model. (a) 1 GHz; (b) 10 GHz.

Coupling Noise in a 3-TS-SWCNTBV Array

- A waveform clock signal with source resistance of 50 Ω is injected into the input port of Signal 1
- The rising/falling time (tr & tf) are 0.4%T0 ; the period is 1 ns and 0.1 ns, respectively; the maximum voltage U0max is 1 V; Mark-Space Ratio (MSR) is 0.5
- The output port of Signal 2 is connected with the load of 50 Ω
- Coupling noise at output port of Signal 2 is captured and compared with the results obtained by the equivalent circuit model
- The peak-to-peak voltage amplitudes of the coupling noise are about 22.4 mV (at 1 GHz) and 91.5 mV (at 10 GHz), respectively
- The amplitude of coupling noise is affected by the rising/falling time very much, which is the reason that it becomes larger at high frequencies

Multiphysics Solution for Almost Carbon Integration



G. Dimitrakakis, *et al.*, *Nano Lett.*, 8(10), 2008.

Thanks

http://coer.zju.edu.cn